Design Guide for Boost Type CCM PFC with ICE2PCSxx

Power Management & Supply

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Design Guide for Boost Type CCM PFC with ICE2PCSxx

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Abstract

ICE2PCS01/02 are the 2nd generation of Continuous Conduction Mode (CCM) PFC controllers, which employ BiCMOS technology. Its control scheme does not need the direct sine-wave sensing reference signal from the AC mains compared to the conventional PFC solution. Average current control is implemented to achieve the unity power factor. In this application note, the design process for the boost PFC with ICE2PCXX is presented and the design details for a 300W output power PFC with the universal input voltage range of 85~265VAC are included.

1 Introduction

The Pin layout of ICE2PCS01 and ICE2PCS02 is shown in Figure 1.

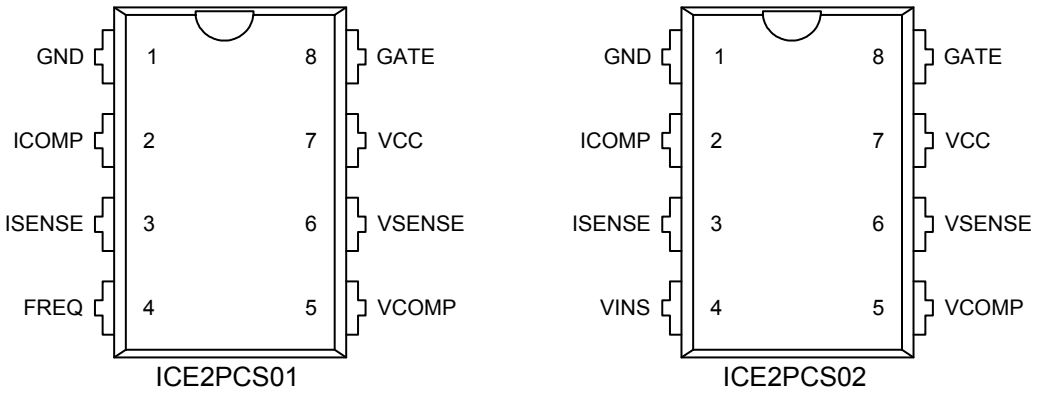


Figure 1 Pin Layout of ICE2PCS01 and ICE2PCS02

From the layout, it can be seen that most of Pins in ICE2PCS02 are the same as ICE2PCS01 except Pin 4. In ICE2PCS01, Pin 4 is to set the switching frequency. However, for ICE2PCS02, Pin 4 is for AC brown out detection and the switching frequency is fixed by internal oscillator at 65kHz. The typical application circuits of ICE2PCS01 and ICE2PCS02 are shown in Figure 2 and Figure 3 respectively.

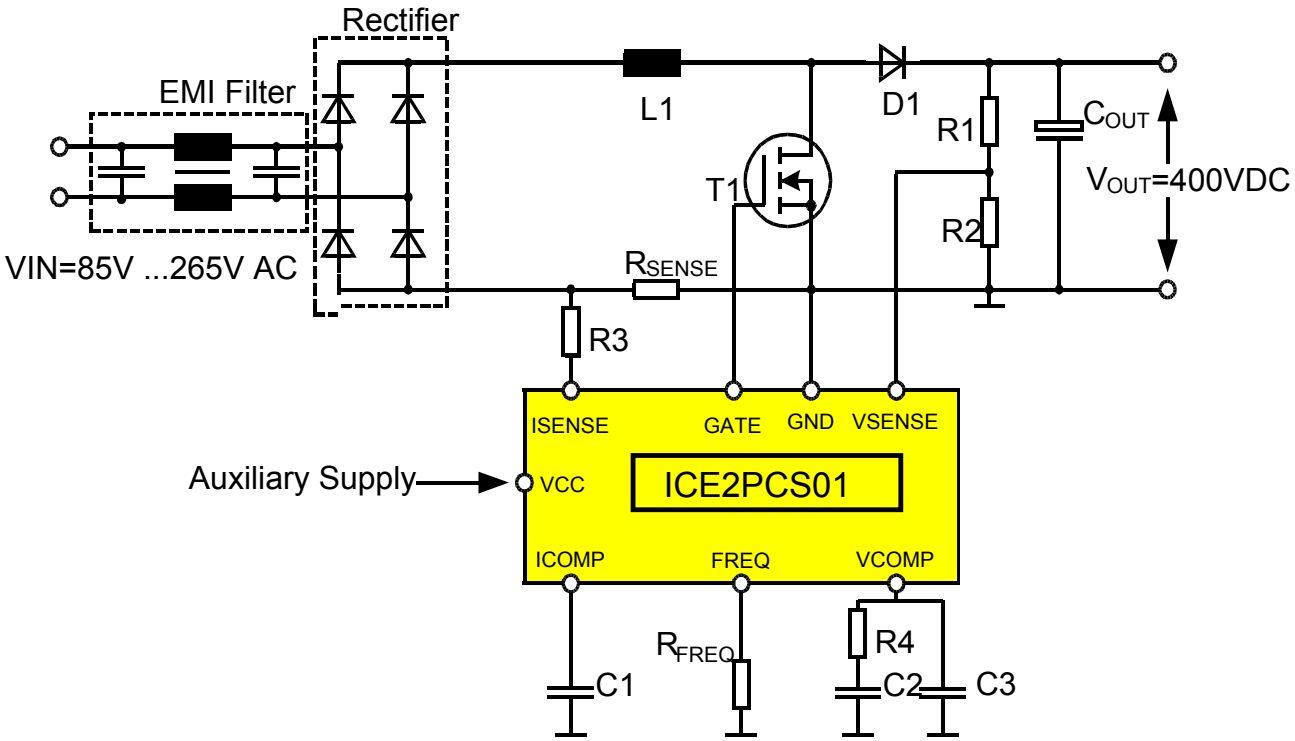


Figure 2 Typical application circuit of ICE2PCS01

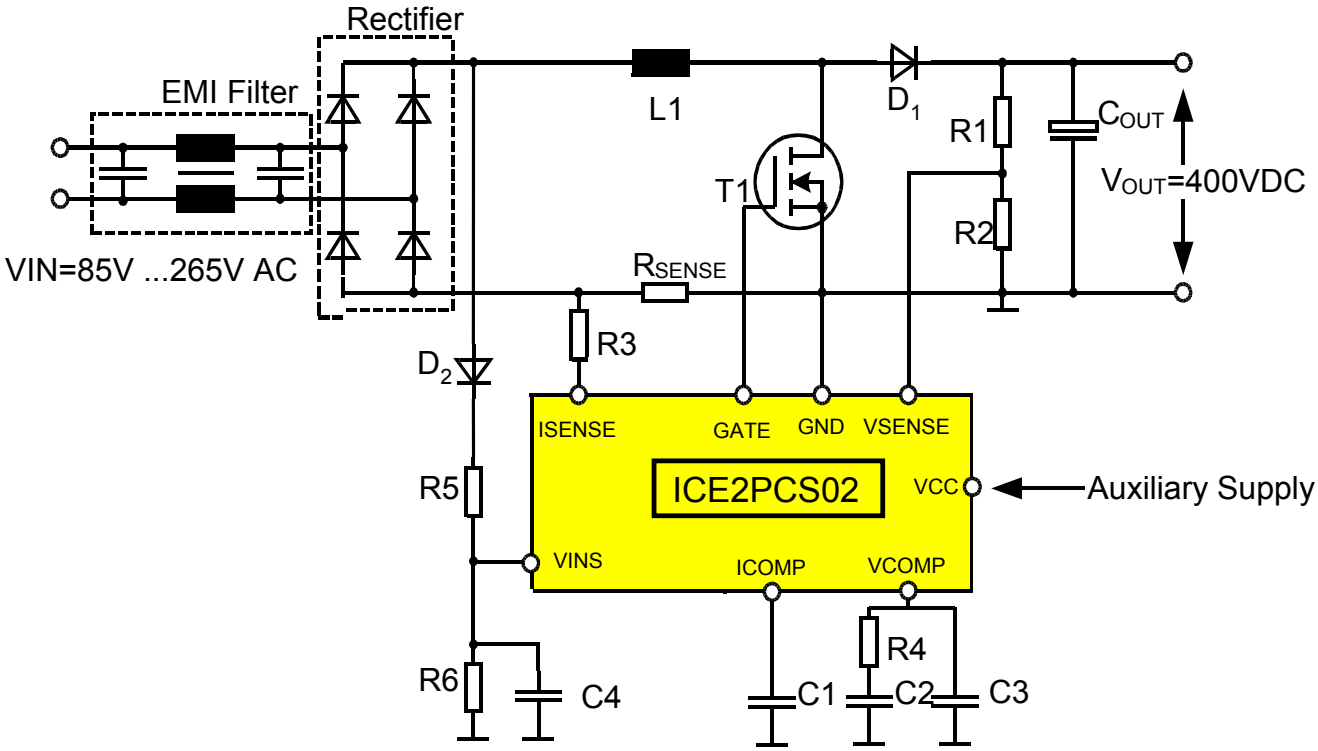


Figure 3 Typical application circuit of ICE2PCS02

2 Boost PFC design with ICE2PCXX

2.1 Target specification

The fundamental electrical data of the circuit are the input voltage range Vin, the output power Pout, the output voltage Vout, the operating switching frequency f_{SW} and the value of the high frequency ripple of the AC line current I_{ripple}. Table 1 shows the relevant values for the system calculated in this Application Note. The efficiency at rated output power Pout is estimated to 91 % over the complete input voltage range.

Input voltage	85VAC~265VAC
Input frequency	50Hz
Output voltage and current	390VDC, 0.76A
Output power	300W
Efficiency	>90% at full load
Switching Frequency	65kHz
Maximum Ambient temperature around PFC	70ºC

Table 1 Design parameter for the proposed design

2.2 Bridge rectifier

In order to obtain 300W output power at 85 V minimum AC input voltage, the maximum input RMS current is

$$I_{in\_RMS} = \frac{P_{out}}{V_{in\_min} \cdot \eta} = \frac{300}{85 \cdot 90\%} = 3.92A \quad (1)$$

and the sinusoidal peak value of AC current is

$$I_{in\_pk} = \sqrt{2} \cdot I_{in\_RMS} = \sqrt{2} \cdot 3.92 = 5.54A \quad (2)$$

For these values a bridge rectifier with an average current capability of 6A or higher is a good choice. Please note here, that due to a power dissipation of approximately

$$P_{BR} = 2 \cdot V_F \cdot I_{in\_RMS} = 2 \cdot 1V \cdot 3.92A = 7.84W \quad (3)$$

the rectifier bridge should be connected to an appropriate heatsink. Assuming a maximum junction temperature T_{Jmax} of 125°C, a maximum ambient temperature T_{Amax} of 70°C, the thermal junction-to-case R_{thJC} of approximate 2.5 K/W and the thermal case to heatsink R_{thCHS} of approximate 1K/W, the heatsink must have a maximum thermal resistance of

$$R_{thHS\_BR} = \frac{T_{J\max} - T_{A\max}}{P_{BR}} - R_{thJC} - R_{thCHS} = \frac{125 - 70}{7.84} - 2.5 - 1 = 3.52K/W \quad (4)$$

2.3 Power MOSFET and Gate Drive Circuit

Due to the switch mode operation, the loss is only valid during the on-time of the MOSFET. The duty cycle of the transistor in boost converters operating in CCM at minimum AC input RMS voltage is

$$D_{on} = 1 - \frac{V_{in\_min}}{V_{out}} = 1 - \frac{85}{390} = 0.782 \quad (5)$$

Since rms-values have the same effect on a system as DC-values, it is possible to calculate a characteristic duty cycle for the rms-value. Therefore, the on-state loss of the MOSFET in CCM-mode at a junction-temperature of 125°C is

$$P_{cond} = I_{in\_RMS}{}^2 \cdot D_{on} \cdot R_{dson(125C)} \quad (6)$$

the MOSFET switching loss can be estimated as

$$P_{SW} = (E_{on} + E_{off}) \cdot f_{SW} \quad (7)$$

where, E_{on} and E_{off} are the switch-on and switch-off energy loss which can be found in MOSFET datasheet, f_{SW} is the switching frequency.

For 300W design, if SPP20N60C3 is used, the conduction loss is

$$P_{cond} = 3.92^2 \cdot 0.782 \cdot 0.42 = 5.05W$$

assuming the switching current is about 6A and gate drive resistance Rg=3.6Ω, then the switching loss is

$$P_{SW} = (0.007mWs + 0.015mWs) * 65kHz = 1.43W$$

the total loss is

$$P_{MOS\_total} = P_{cond} + P_{SW} = 6.48W \quad (8)$$

the required heatsink for the MOSFET is

$$R_{thHS\_MOS} = \frac{T_{J\max} - T_{A\max}}{P_{MOS\_total}} - R_{thJC\_MOS} - R_{thCHS} = \frac{125-70}{6.48} - 0.6 - 1 = 6.89K/W \quad (9)$$

R_{thCHS} is the Rth of the insulation pad between MOSFET and heatsink.

Gate drive resistance is used to drive MOSFET as fast as possible but also keep dv/dt within EMI specification. In this 300W example, 3.6Ω gate resistor is chosen for SPP20N60C3 MOSFET.

Beside gate drive resistance, one 10kΩ resistor is also commonly connected between MOSFET gate and source to discharge gate capacitor.

2.4 Boost Diode

The boost diode D1 has big influence on the system's performance due to the reverse recovery behaviour. So the Ultra-fast diode with very low t_{rr} and Q_{rr} is necessary to reduce the switching loss. The new diode technology of silicon carbide (SiC) Schottky shows its outstanding performance with almost no reverse recovery behaviour. The switching loss due to the boost diode can be ignored with SiC Schottky diode. Only conduction loss is calculated as below.

$$P_{diode} = V_F \cdot I_{in\_RMS} \cdot (1 - D_{on}) = 2V \cdot 3.92A \cdot (1 - 0.782) = 1.71W \quad (10)$$

To decide the current rating of a SiC diode, there is a rule of thumb - the SiC diode can handle output power Pout of 100 W to120 W in a CCM-PFC-system per one rated ampere. For example, the SDT04S60 from Infineon Technologies is rated at a forward current IF = 4 A, so it is capable for a system of Pout = 4*100 W = 400 W system in minimum. Therefore, this diode should be suitable for the proposed design.

The required heatsink for boost diode is

$$R_{thHS\_diode} = \frac{T_{J\max} - T_{A\max}}{P_{diode}} - R_{thJC\_diode} - R_{thCHS} = \frac{125-70}{1.71} - 4.1 - 1 = 27.06K/W \quad (11)$$

The SiC boost diodes often have a poor surge current handling capability. Therefore a so called bypass diode is necessary such as the diode D3 as Figure 4. For the proposed system, 1N5408 is suitable.

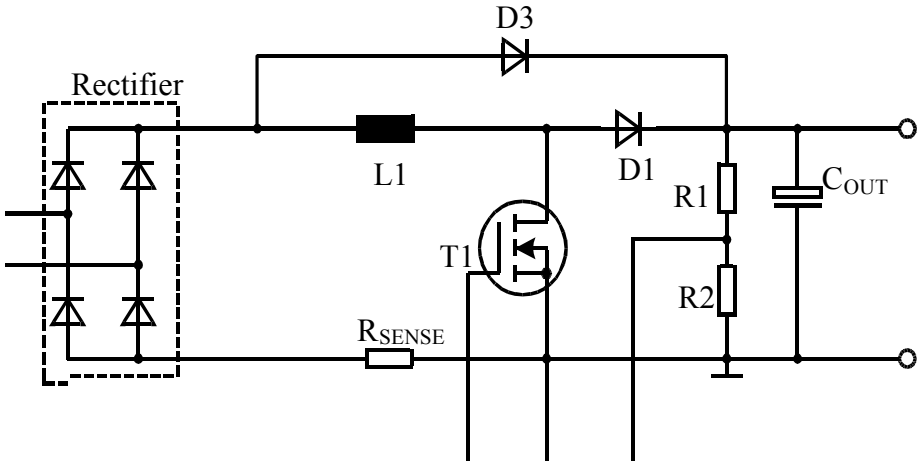


Figure 4 inrush current bypass diode

2.5 Boost inductor

The peak current that the inductor must carry is the peak line current at the lowest input voltage plus the high frequency ripple current. The high frequency ripple current peak to peak, I_{HF}, can be related to maximum input power and minmum input voltage as equation below.

$$I_{HF} = k \cdot \sqrt{2} \cdot \frac{P_{in\_\max}}{V_{in\_\min}} \tag{12}$$

Where, k must be kept reasonably small, and is usually optimized in the range of 15% to 25% for cost effective design based on the current magnetic component status. If k is too high, the larger AC input filter is required to filter out this ripple noise. If k is too low, the value of the inductance is too large and leads to big size of the magnetic core.

For example, we choose k = 22%, then,

$$I_{HF} = 22\% \cdot \sqrt{2} \cdot \frac{P_{in\_\max}}{V_{in\_\min}} = 1.2A$$

The peak current passing through inductor is

$$I_{L\_pk} = I_{in\_peak} + \frac{I_{HF}}{2} = 5.54 + \frac{1.2}{2} = 6.14A \tag{13}$$

The boost choke inductance must be

$$L_{boost} \geq \frac{D \cdot (1-D) \cdot V_{out}}{I_{HF} \cdot f_{SW}} \tag{14}$$

D=0.5 will generate the maximum value for the above equation.

$$L_{boost} \geq \frac{0.5 \cdot (1-0.5) \cdot 390V}{1.2A \cdot 65kHz} = 1.25mH$$

The magnetic core of the boost choke can be either magnetic powder or ferrite material.

(1) sendust powder toroid core

The required effective magnetic volume of the core, V_e, is

$$V_e \geq \mu_r \mu_0 L_{boost} (\frac{I_{L\_pk}}{B_{\max}})^2 = 125 \cdot 1.257e-6 \cdot 1.25mH (\frac{6.14A}{0.8T})^2 = 11.6e-6m^3 = 11.6cm^3 \quad (15)$$

where, μ_r is the relative permeability of the material. It should be noted that μ_r changes with different DC magnetizing force H, and so does the inductance. As an example, Figure 5 illustrates the relationship between the Percent Permeability and the DC Magnetizing Force H.

μ_0 in (15) is the magnetic field constant which is equal to 1.257e-6; B_{max} is the maximum magnetic flux density for the selected magnetic material (for sendust, B_{max} is up to 0.8T.)

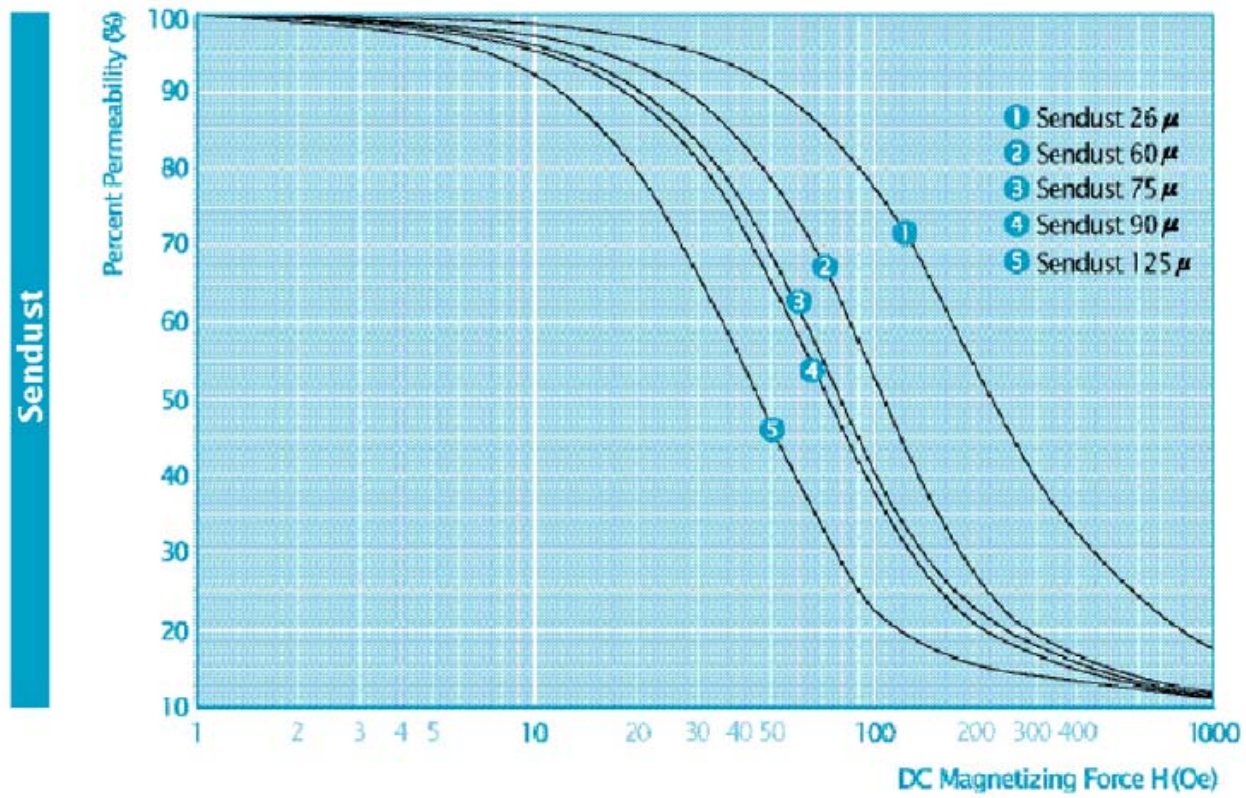


Figure 5 Percent Permeability and DC Magnetizing Force H (from Changsung)

Select a core with similar Ve value from the magnetic core datasheet. For example, the core type CS468125 from Chang Sung Corporation is selected. The parameters of CS468125 are V_e=15.584cm^3, A_e=1.34cm^2, C=11.63cm, μ_r=125. The turn number of the boost choke winding is

$$N_{toroid\_boost} = \sqrt{\frac{L_{boost} \cdot C}{\mu_r \mu_0 A_e}} = 83 \quad (16)$$

where, C is the magnetic path length and A_e is the effective magnetic cross section area.

To check the actual μ_r at low line, maximum power, the DC Magnetizing Force H is calculated

$$H = \frac{NI_{in\_pk}}{C} = 50(Oe)$$

Then μ_r = 125 * 50% = 62.5 according to Figure 5. The actual inductance can be re-calculated as $L_{boost} = \frac{N^2 \mu_r \mu_0 A_e}{C} = 0.625mH$. Hence, the corresponding ripple current will be higher than the previously assumed value.

The copper loss of the winding wire can be calculated on I_{in_RMS}.

$$P_{L\_boost} = I_{in\_RMS}^{\ 2} \cdot R_{L\_boost} \tag{17}$$

Select the proper wire type to fullfil the loss and thermal requirement for the choke.

(2) ferrite core

To make sure the ferrite core will not go into saturation, the turn number of the boost choke winding with ferrite core is

$$N_{ferrite\_boost} \geq \frac{I_{L\_pk} \cdot L_{boost}}{B_{\max} \cdot A_{\min}} \tag{18}$$

where, B_{max} is up to 0.3T according to ferrite material specification; A_{min} is the minimum magnetic cross section area.

The winding wire copper loss calculation is the same as in the above section of sendust powder toroid core.

2.6 AC line current filter

As decribed in section 2.5, there is high frequency ripple current peak to peak I_{HF} passing through boost choke. This ripple will also go into AC line power network. The current filter is necessary to reduce the amplitude of high frequency current component. The filtering circuit consists of a capacitor and an inductor as shown in Figure 6.

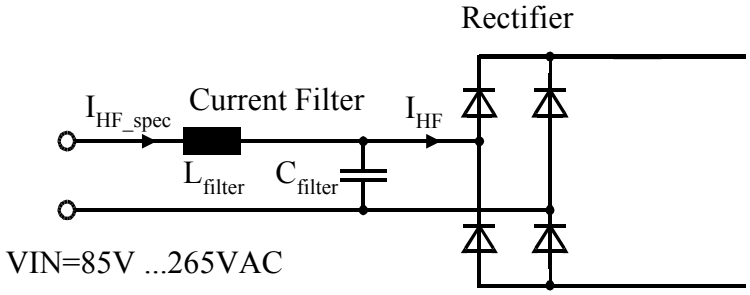


Figure 6 AC line current filter

The required L_{filter} is

$$L_{filter} \geq \frac{\frac{I_{HF}}{I_{HF\_spec}} + 1}{(2\pi f_{SW})^2 C_{filter}} \tag{19}$$

normally there is one EMI X2 capacitor which can act as C_{filter}. In this example, if we define I_{HF_spec} as 0.2A peak to peak and asumming X2 capacitance 0.47μF, then

$$L_{filter} \geq \frac{\frac{1.2A}{0.2A} + 1}{(2\pi \cdot 65kHz)^2 \cdot 0.47\mu F} = 89\mu H$$

The leakage inductance of EMI common mode choke can be used for current filter. If the leakage inductance is large enough, no need to add the additional differential mode inductor for filtering. Otherwise, a current filter choke is necessary. The calculation method for the current filter choke is the same as for boost choke.

2.7 Boost Output Bulk Capacitance

The bulk capacitance has to fullfil two requirements, output double line frequency ripple and holdup time.

(1) output double line frequency ripple limit.

The inherent PFC always presents 2*f_L ripple. The amplitude of ripple voltage is dependant on output current and bulk capacitance as below.

$$C_{out} \geq \frac{I_{out}}{\pi \cdot 2 * f_L \cdot V_{out\_ripple\_pp}} \tag{20}$$

where, I_{out} is the PFC output current, $V_{out\_ripple\_pp}$ is the output voltage ripple (peak to peak), and f_L is the AC line frequency.

Please note that ICE2PCXX has enhance dynamic block which is active when Vout exceed ±5% of regulated level. The enchanc dynamic block should be designed to work only during load or line change. During steady state with constant load, the enhance dynamic block should not be triggered, otherwise THD will be deteriorated. That means the target $V_{out\_ripple\_pp}$ must be lower than 10% of V_{out}. For this example, Vout=390VDC, then $V_{out\_ripple\_pp}$ must be lower than 39V. if we define $V_{out\_ripple\_pp}$=12V, then

$$C_{out} \geq \frac{I_{out}}{\pi \cdot 2 \cdot f_L \cdot V_{out\_ripple\_pp}} = 220\mu F \tag{21}$$

(2) holdup time requirement

After the PFC stage, there is commonly a PWM stage to provide isolated DC output for end user. Some applications, especially computing, have the holdup time requirement. It means that PWM stage should be able to provide the isolated output even if AC input voltage become zero for a short holdup time. The common specification for this holdup time is 20ms. If minimum input voltage for PWM stage is defined as 250VDC, then the bulk capacitance will be

$$C_{out} \geq \frac{2 \cdot P_{out} \cdot t_{holdup}}{V_{out}^{\ 2} - V_{out\_\min}^{\ 2}} = \frac{2 \cdot 300W \cdot 20ms}{390^2 - 250^2} = 134\mu F \tag{22}$$

the final C_{out} capacitance should be higher value calculated from the above two requirements.

2.8 Current Sense Resistor

The current sense resistance is calculated based on the IC soft over current control threshold and peak current carried by boost choke.

When the Isense signal reaches the soft over control threshold, IC will reduce the internal control voltage and accordingly the duty cycle is reduced in the following cycles. Finally the boost choke current is limited. According to IC datasheet, soft over current control threshold is -0.68V maximum. So the current sense resistor should be

$$R_{sense} \leq \frac{0.68V}{I_{L\_pk}} = \frac{0.68V}{6.14A} = 0.11\Omega \tag{23}$$

According to Figure 2 and Figure 3, the transistor current as well as the diode current flows through R_{sense}. That means, when AC is powered up, a large negative voltage drop at R_{sense} will be observed when large inrush current in the range of about 150 A to 200 A flows through the resistor. It is therefore necessary to limit the current into Pin 2 (ISENSE) to 1 mA, which is realized with resistor R3. A value of R3 = 220Ω is sufficient for this resistor.

2.9 Output voltage sensing divider

The output voltage is set with the voltage divider represented by R_1 and R_2 in Figure 2 and Figure 3. First, choose the value of the lower resistor R_2. Then the value of the upper resistor R_1 is

$$R_1 = \frac{V_{out} - V_{ref}}{V_{ref}} \cdot R_2 \tag{24}$$

where, Vref is IC internal reference voltage for voltage sensing, 3V typical.

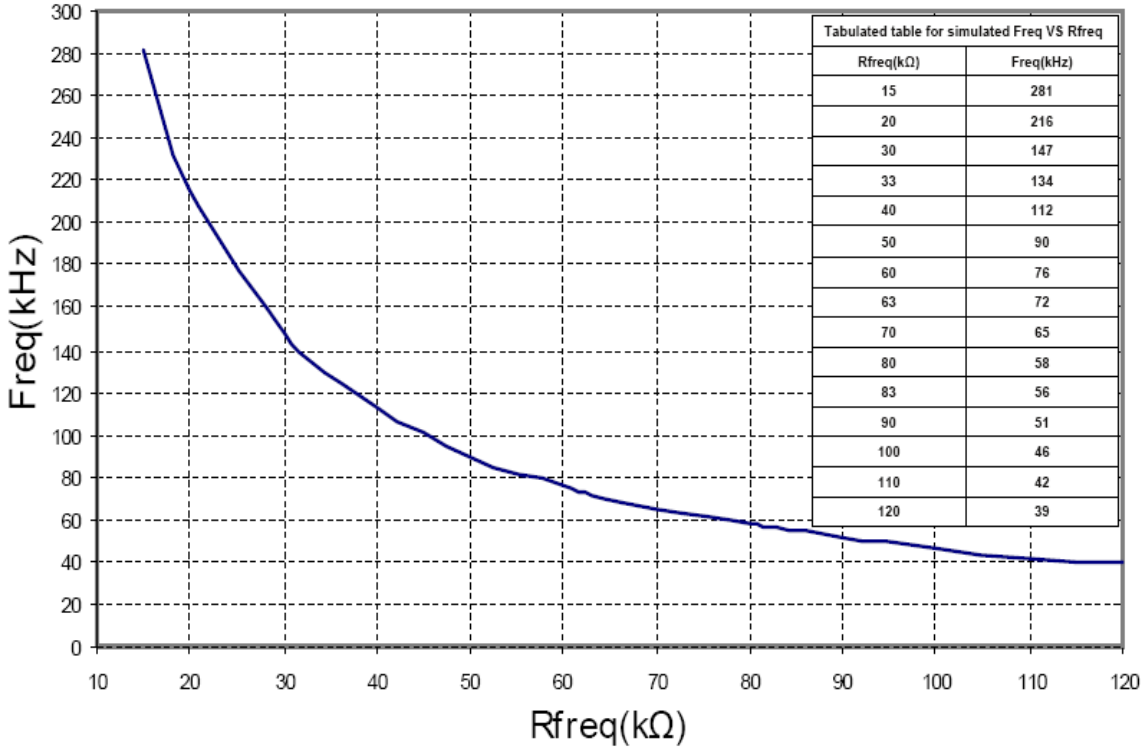
If R_2=6kΩ,

$$R_1 = \frac{390 - 3}{3} \cdot 10k\Omega = 774k\Omega$$

It is recommended to take resistor values with a tolerance of 1% for R_1 and R_2. Due to the voltage stress of R1, it is recommended to split this value into few resistors in series.

2.10 Frequency setting (only for ICE2PCS01)

The frequency of the ICE2PCS01 is adjustable in the range of 50 kHz up to 250 kHz. The external resistor R_{FREQ} according to Figure 7 programs a current which controls the oscillator.



Tabulated table for simulated Freq VS Rfreq

Rfreq(kΩ)	Freq(kHz)
15	281
20	216
30	147
33	134
40	112
50	90
60	76
63	72
70	65
80	58
83	56
90	51
100	46
110	42
120	39

Figure 7 Resistor-frequency characteristic

2.11 AC Brown-out Shutdown (only for ICE2PCS02)

Brown-out occurs when the input voltage VAC falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the VCC has not entered into the VCCUVLO level yet. For a system without input brown out protection (IBOP), the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current and lead to over heat of MOSFET and boost diode. ICE2PCS02 provides a new IBOP feature whereby it senses directly the input voltage for Input Brown-Out condition via an external resistor/capacitor/diode network as shown in Figure 8. This network provides a filtered value of VIN which turns the IC on when the voltage at Pin 4 (VINS) is more than 1.5V. The IC enters into the standby mode and gate is off when VINS goes below 0.7V. The hysteresis prevents the system to oscillate between normal and standby mode.

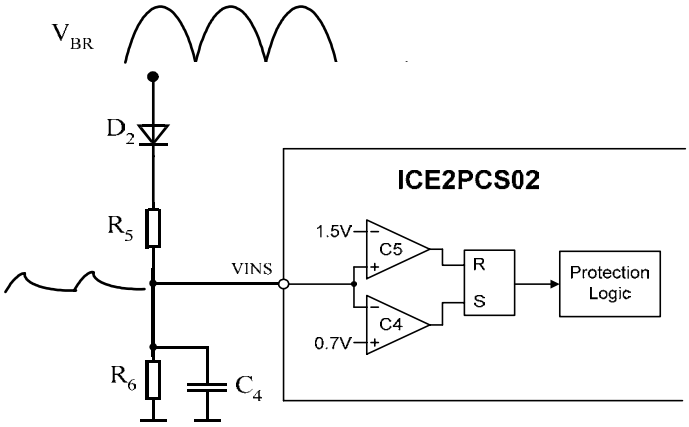


Figure 8 Block diagram of voltage loop

Because of the high input impedence of comparator of C4 and C5, R5 can be high ohmic resistance to reduce the loss. From the datasheet, the bias current on VINS Pin is 1μA maximum. In order to have the design consistence, the current passing through R5 and R6 has to be much higher than this bias current, for example 6μA. Then R6 is:

$$R_6 = \frac{0.7V}{6uA} = 117k\Omega \tag{25}$$

R6 is selected 120KΩ. R5 is selcted by

$$R_5 = \frac{\sqrt{2} \cdot V_{AC\_on} - 1.5V}{1.5V} \cdot R_6 \tag{26}$$

where, V_{AC_on} is the minimum AC input voltage (RMS) to start PFC, for example 70VAC.

$$R_5 = \frac{\sqrt{2} \cdot 70V - 1.5V}{1.5V} \cdot 120k\Omega = 7.8M\Omega$$

Due to the voltage stress of R_5, it is recommended to split this value into few resistors in series.

C_4 is used to modulate the ripple at the VINS pin. The timing diagram of VINS pin when IC enters brown-out shutdown is shown in Figure 9.

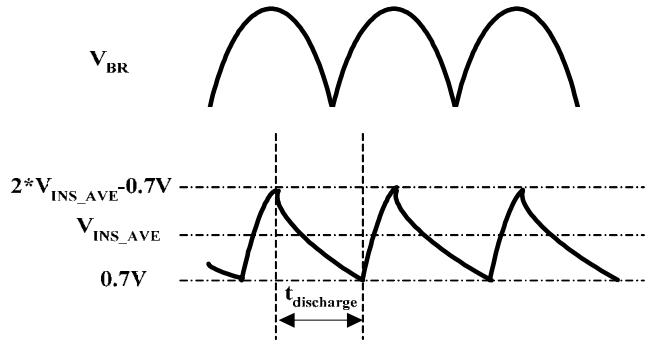


Figure 9 Timing diagram of VINS Pin when IC enters brown-out shutdown

If the bottom level of the ripple voltage touches 0.7V, PFC is in standby mode and gate is off. The ripple voltage defines PFC brown out off threshold of AC input voltage (RMS), V_{AC_off}. C_4 can be obtained from the following equation. Assuming $V_{INS\_AVE} = \frac{R_6}{R_5 + R_6} \cdot V_{AC\_off}$, where, V_{AC_off} is the maximum AC input voltage (RMS) to switch off PFC, for example 65VAC.

$$(2 \cdot \frac{R_6}{R_5 + R_6} \cdot V_{AC\_off} - 0.7) \cdot e^{-\frac{t_{discharge}}{R_6 C_4}} = 0.7V \tag{27}$$

assuming $t_{discharge}$ is equal to half cycle time of line frequency, ie. $t_{discharge} = \frac{1}{2 f_L}$, then

$$C_4 = \left(2 f_L R_6 \ln \frac{2 \cdot \frac{R_6}{R_5 + R_6} V_{AC\_off} - 0.7V}{0.7V} \right)^{-1}$$

$$C_4 = \left(2 \cdot 50Hz \cdot 120k\Omega \ln \frac{2 \cdot \frac{120k\Omega}{7.8M\Omega + 120k\Omega} 65V - 0.7V}{0.7V} \right)^{-1} = 140nF \tag{28}$$

2.12 IC supply

The IC supply voltage operating range is 11~26V.

There are two stages during IC turned on. First Vcc capacitor is charged from 0V to 7V, the IC internal regulator block starts to reset voltage at all external pins. The reset process will take about 10us. And then when Vcc voltage is charged to Vcc_on threshold, IC starts the soft start with gate switching. In the case of Vcc decoupling capacitance is too low such as 0.1uF, Vcc voltage may be charged up too fast and the time interval from Vcc=7V to Vcc_on is less than the reset time. Then the IC will not go through a proper soft start as the voltages at IC pins are not yet properly reset. To avoid such a problem, the delay circuitry is needed.

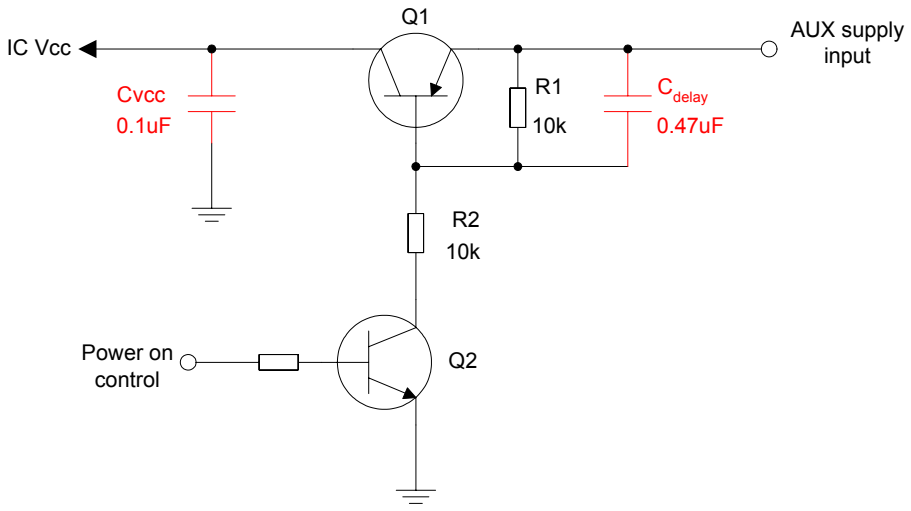


Figure 10 Vcc supply circuitry

Figure 10 is a typical circuitry to supply PFC controller. Q2 is NPN transistor and controlled by external "Power on" signal. When "Power on" signal is "high", Q2 is turned on provides base current for Q1. Q1 is turned on accordingly to supply auxiliary power to IC Vcc. The reset delay time is adjustable by changing the RC time constant of R1, R2 and C_{delay}. The recommended values are shown in Figure 10 as 10kΩ, 10kΩ and 0.47uF respectively.

The same reset process also happens during IC power down when Vcc is discharged from Vcc_off to 7V. The reset time for power down is around 200us. Because IC is in power down mode with very low current consumption, typically 300uA only, the required Vcc capacitance for power down reset can be calculated as:

$$C_{VCC} \geq \frac{I_{power\_down\_max} \cdot t_{reset}}{V_{cc\_off\_min} - V_{reset}} = \frac{650\mu A \cdot 200\mu s}{10.4V - 7V} = 38.2nF \quad (29)$$

So the common Vcc decoupling capacitance 0.1uF is enough for reset delay requirement.

2.13 PCB layout guide

In order to avoid crosstalk on the board between power and signal path, and to keep the IC GND pin as "clean" from noise as possible, the PCB layout for GND must be taken care of properly. Below are some suggestions for GND connection and Figure 11 below illustrates as a good example.

(1) Star connection rule for main power stage GND: the PCB tracks of MOSFET source, output load GND, IC auxiliary supply GND and shunt resistor are separated and connected together at bulk capacitor negative Pin.

(2) Star connection rule for small signal IC GND: the IC external components which need to be connected to the small signal GND bus highlighted in red color. Such GND bus is connected to IC GND Pin.

(3) Connection between main power stage GND and small signal IC GND: in Figure 11, a single PCB track in pink color directly connect IC GND pin to power stage star connection point - bulk capacitor negative. This is to ensure that the voltage between IC Isense Pin and IC GND Pin does not observe the switching rectangular noise current. The dark green and blue tracks denote for flowing paths of high frequency rectangular switching current.

(4) Vcc decoupling capacitor Cvcc: the decoupling capacitor need to be placed close to IC Vcc and GND Pins as much as possible. The GND track of Cvcc (green color in Figure 11) should be connected at the point on the single PCB track connecting between IC GND Pin and power GND point so that the large gate charging current will not pass through the small signal GND bus.

(5) Vsense capacitor Cvsense: to reduce noise in Vsense Pin, small capacitor up to 0.1uF can be added between Vsense Pin and small signal GND bus.

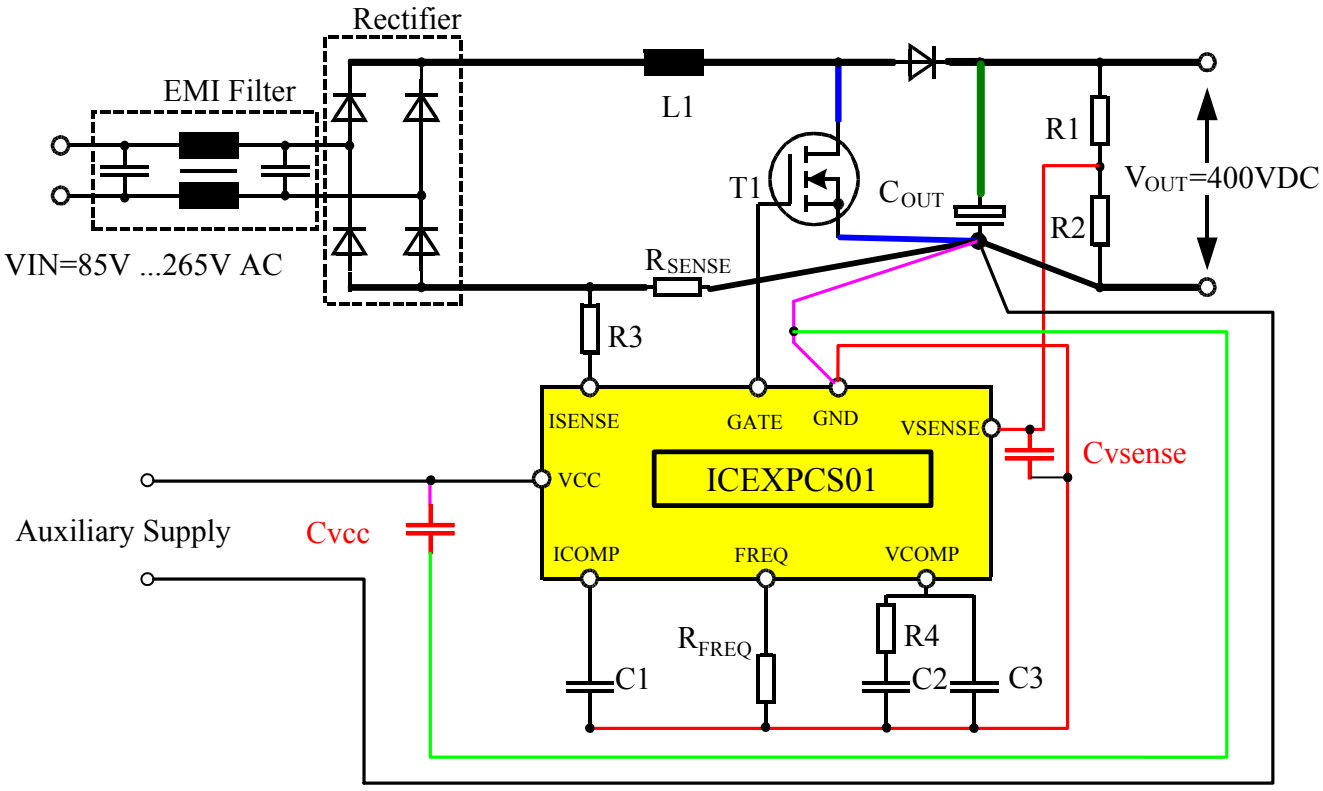
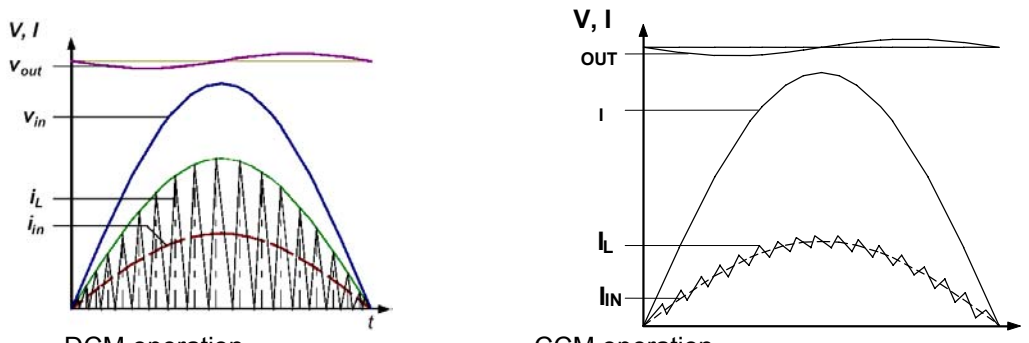


Figure 11 Good PCB layout illustration

3 Voltage loop and current loop compensation

This section provides a model and a tool for evaluating and improving the control loop characteristics of ICE2PCS02-based PFC pre-regulators in boost topology. The goal is not only to ensure a narrow bandwidth in order to achieve a high Power Factor, but also to have enough phase margin so as to make sure the system is stable over a large range of operating conditions. The design example is demonstrated as well.

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produce radiated and conducted electromagnetic interference, leads to poor utilization of the capacity of the power sources. In compliance with IEC 61000-3-2 harmonic regulation, active power factor correction (PFC) circuit is getting more and more attention in recent years. For low power up to 200W, discontinuous conduction mode (DCM) PFC is popular due to its lower cost. Furthermore, there is only one control loop, i.e. voltage loop, in its transferring control blocks. The design is easy and simple for DCM operation. However, due to its inherent high current ripple, DCM is seldom to be used for high power applications. In high power applications, continuous conduction mode (CCM) PFC is more attractive.



DCM operation CCM operation

Figure 12 DCM and CCM PFC principle

3.1 How to achieve PFC function without sinusoidal reference sensing

3.1.1 Boost converter modeling

Figure 13 shows the inductor current waveform for boost converter operating in continuous conduction mode.

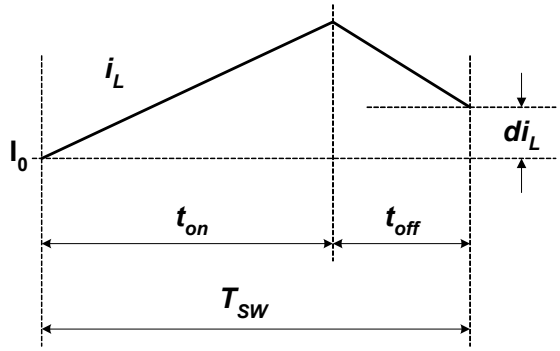


Figure 13 inductor current waveform of boost converter operating in CCM mode

assuming Vin is boost converter input DC voltage, Vout is the boost converter output voltage, L is the boost choke inductance, ton is the on time duration in one switching cycle, toff is the off time duration in one switching cycle, doff is the off time duty cycle and Tsw is the time duration in one switching cycle.

During “on” interval,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{30}$$

During “off” interval,

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{31}$$

And then the boost inductor current variation after one switching cycle is:

$$di_L = \frac{V_{in}}{L} \cdot t_{on} + \frac{V_{in} - V_{out}}{L} \cdot t_{off} = \frac{V_{in} - V_{out} \cdot d_{off}}{L} \cdot T_{SW} \tag{32}$$

The instant boost inductor current after n switching cycle is:

$$i_{L\_n} = i_{L\_n-1} + \frac{V_{in\_n} - V_{out\_n} \cdot d_{off\_n}}{L} \cdot T_{SW} \tag{33}$$

3.1.2 PFC IC control principle with boost topology

PFC IC control block is inserted in boost converter as shown in Figure 14.

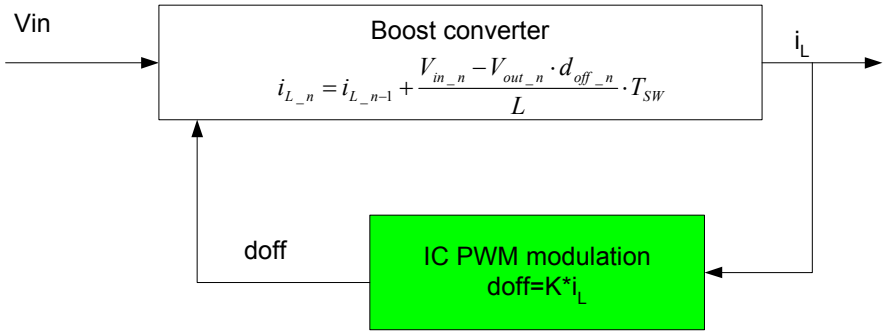


Figure 14 PFC current loop principle

IC senses boost inductor average current, and calculate the off duty cycle to be proportional to inductor current, and then send such off duty cycle back to boost converter. The negative feedback loop can be seen from Figure 14. A small disturb increasing on i_L will result in a little bit increasing on off duty cycle. The increasing off duty cycle will lead to decreasing of i_L after processing by boost converter. In the stead state,

$$V_{in} = V_{out} \cdot d_{off} = V_{out} \cdot K \cdot i_L \quad (34)$$

Where, K is the modulation gain defined by IC. It can be seen that boost inductor current shape follows AC input voltage and it is how PFC function to be achieved.

In the following sections, detail mathematical analysis of current loop and voltage loop will be described and the transfer function for each block is given in order to design IC external compensation network components.

3.2 Current Loop Regulation and Transfer Function

The detail block diagram of current loop for ICE2PCS02 is shown in the Figure 15. The boost converter stage K_{boost} is elaborated in S-plane.

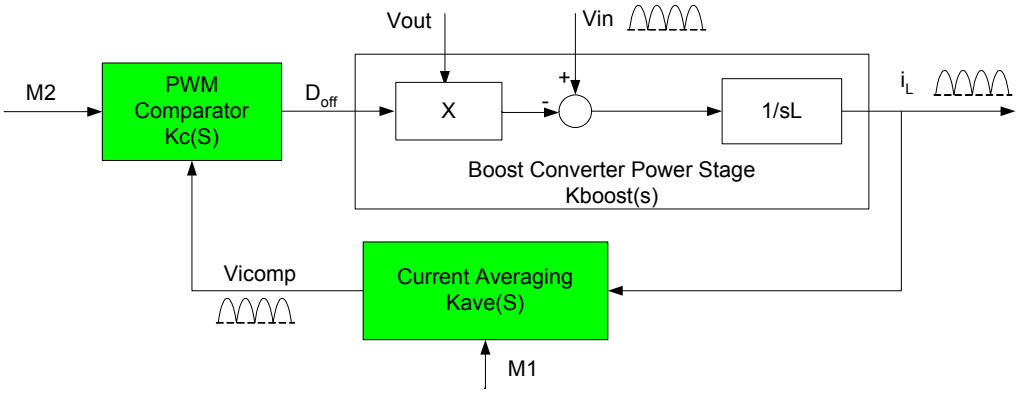


Figure 15 Block diagram of current loop

3.2.1 Current Averaging Circuit

IC sense the boost inductor current via shunt resistor Rsense as shown in Figure 2. The sensing signal is sent to Isense Pin. As the voltage in Isense Pin is negative signal together with switching ripple, IC need to do signal averaging and convert the polarity to positive for following PWM modulation blocks. The output of averaging block is Vicomp voltage at Icomp Pin. the block diagram of current averaging block is shown in Figure 16.

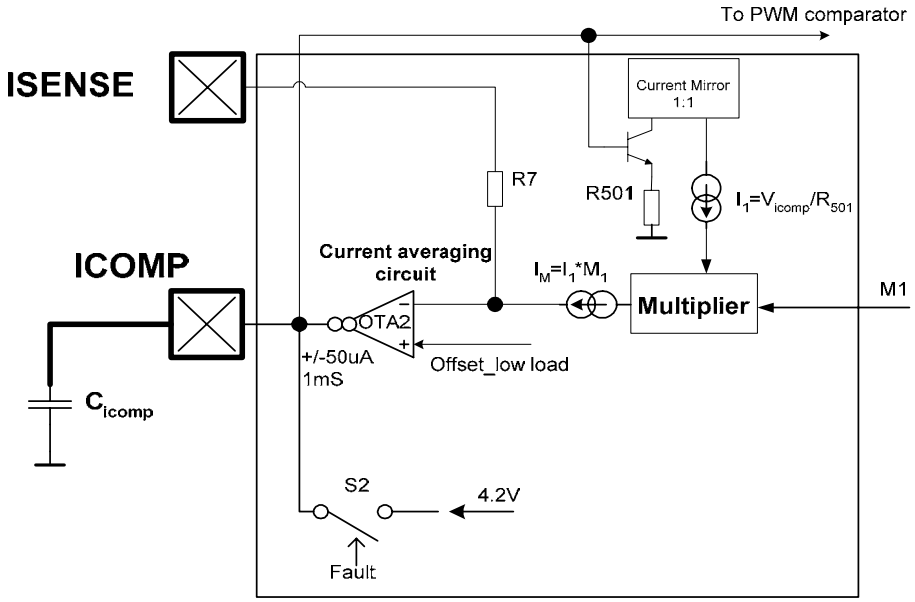


Figure 16 current averaging block diagram

The transfer function of averaging circuit block can be derived as below.

$$K_{AVE}(s) = \frac{V_{icomp}}{i_L} = \frac{\frac{K_1 R_{sense}}{M_1}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \tag{35}$$

where, K_1 is a ratio between R501 and R7 which is equal to 4, C_{icomp} is the capacitor at Icomp Pin, g_{OTA2} is the trans-conductance of the error amplifier of OTA2 for current averaging, typical 1.0mS as shown in Datasheet, M1 is the variable controlled by voltage loop.

The function of the averaging circuit is to filter out the switching current ripple. So the corner frequency of the averaging circuit f_{AVE} must be lower than the switching frequency f_{SW}. Then,

$$C_{icomp} \geq \frac{g_{OTA2} M_1}{K_1 \cdot 2\pi f_{AVE}} \tag{36}$$

3.2.2 PWM comparator block

The averaged Vicomp signal is sent to PWM comparator block and compared with internal triangular ramp signal to derive duty cycle. The timing diagram of this block is shown in Figure 17.

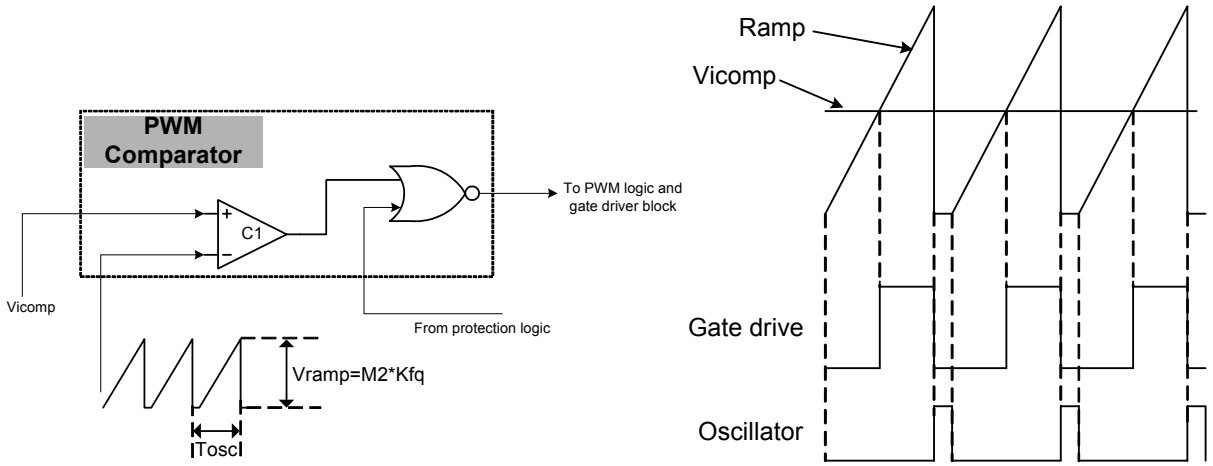


Figure 17 The block diagram and timing sequence of PWM comparator block

The operating principle is explained as following. Gate output is in “low” state in the beginning of the each cycle. Gate output is turned to “high” at the intersection of the triangular ramp signal and Vicomp signal. Gate output is turned to “low” by oscillator synchronous signal. Based on the operating principle, the transfer function of $K_C(s)$ is:

$$K_C(s) = \frac{d_{off}}{V_{icomp}} = \frac{1}{K_{FQ} M_2} \tag{37}$$

Where, K_{FQ} is a design constant which is equal to 9.183, M_2 is the variable controlled by voltage loop.

3.2.3 Boost converter stage

The transfer function of boost converter stage $K_{Boost}(s)$ can be obtain via State-Space Averaging method. Combining equation (30) and (31) by state –space averaging,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} d_{on} + \frac{V_{in} - V_{out}}{L} d_{off} = \frac{V_{in} - V_{out} d_{off}}{L} \tag{38}$$

Make Laplace transformation for equation (38) with assuming Vin and Vout are constant for current loop analysis,

$$i_L(s) = (V_{in} - V_{out} d_{off}(s)) \frac{1}{sL} \tag{39}$$

The equation (39) has been described in current loop block diagram in Figure 15. **Although Vin is not physically sensed by circuit, the input sinusoidal signal is presented in transfer functions only if boost topology is applied.**

3.2.4 Open loop transfer function gain for current loop

The open loop gain of current regulation loop is:

$$G_C(s) = K_{AVE}(s) K_C(s) \frac{V_{out}}{sL} = \frac{\frac{K_1 R_{sense} V_{out}}{K_{FQ} M_1 M_2 L}}{s(1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}})} \tag{40}$$

The selected C_{icomp} must also meet the requirement that the cross over frequency of the current loop f_C is much lower than the switching frequency f_{SW}.

3.2.5 Steady state solution of I_L

Solving the current loop in Figure 15,

$$i_L(s) = (V_{in} - V_{out} d_{off}(s)) \frac{1}{sL} = (V_{in} - V_{out} K_C(s) K_{AVE}(s) i_L(s)) \frac{1}{sL}$$

$$i_L(s) = \frac{\frac{V_{in}}{sL}}{1 + \frac{V_{out} K_C(s) K_{AVE}(s)}{sL}} = \frac{\frac{V_{in}}{sL}}{1 + G_C(s)} \tag{41}$$

For AC line frequency which is much lower than f_C, then $|G_c(s)| >> 1$

$$i_L(s) = \frac{\frac{V_{in}}{sL}}{1 + G_C(s)} \approx \frac{\frac{V_{in}}{sL}}{G_C(s)} = \frac{\frac{K_{FQ} M_1 M_2 V_{in}}{K_1 R_{sense} V_{out}}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \tag{42}$$

For AC line frequency which is also much lower than f_{AVE}, $\left| s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}} \right| << 1$, then the steady state I_L can be derived as

$$I_L = \frac{K_{FQ} M_1 M_2 V_{in}}{K_1 R_{sense} V_{out}} \tag{43}$$

from the above steady state solution of I_L, it can be seen that the choke current I_L is always following input voltage V_{in}. This is how PFC function is achieved.

3.3 Voltage Loop Compensation

The control loop block diagram for ICE2PCS02 based CCM PFC is shown in Figure 18 and Figure 19. There are four blocks in the loop. IC PWM Modulator $G_2(s)$ has been discussed in above Section 3. the rest of them are Error Amplifier $G_1(s)$, nonlinear block $G_{NON}(s)$, boost converter output stage $G_3(s)$ and Feedback Sensing $G_4(s)$.

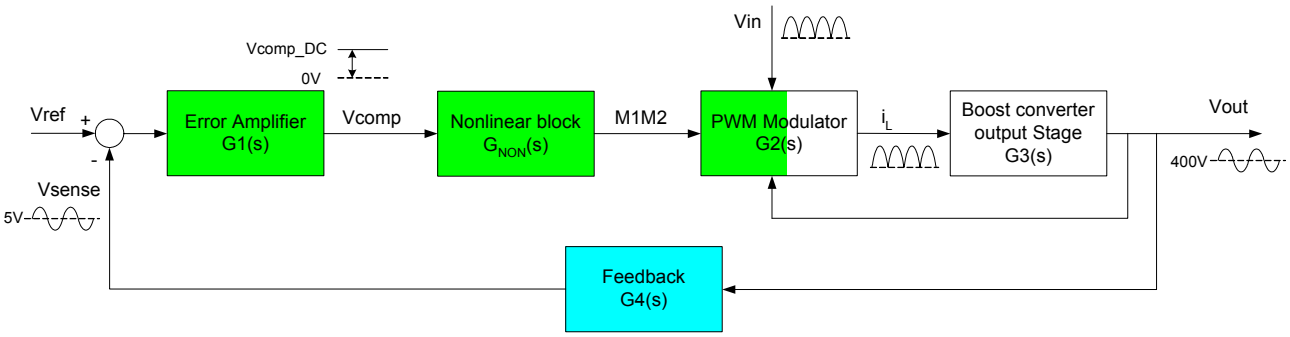


Figure 18 Large signal modeling of voltage loop

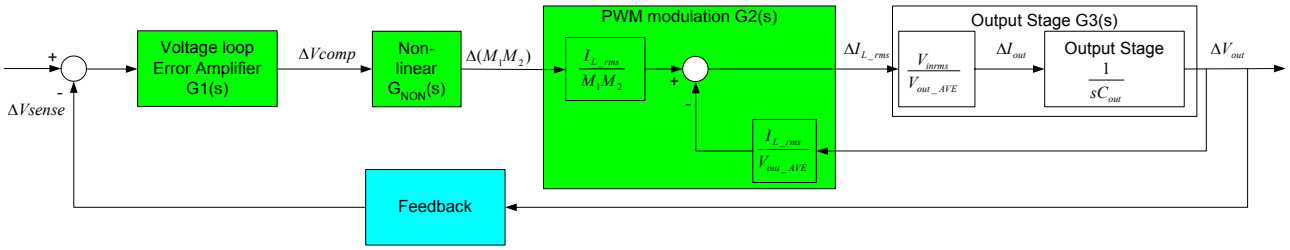


Figure 19 Small signal modeling of voltage loop

3.3.1 Boost converter output stage $G_3(s)$

Boost converter output stage is described as influencing of variation on i_L to bulk output voltage Vout. The transfer function of power stage, $G_3(s)$, is separated to two stages as:

$$G_3(s) = \frac{\Delta V_{out}}{\Delta I_{L\_rms}} = \frac{\Delta V_{out}}{\Delta I_{out}} \cdot \frac{\Delta I_{out}}{\Delta I_{L\_rms}} \tag{44}$$

where V_{out} is the DC output voltage, I_{out} the DC output current and I_{L_rms} is the boost inductor current.

3.3.1.1 ΔV_{out} / ΔI_{out}

Under the above assumption, the power stage can be modeled as illustrated in Figure 20: a controlled current source (with a shunt resistor Re) that drives the output bulk capacitor C_{out} and the load resistance Rout (= Vout / Iout). The zero due to the ESR associated with C_{out} is far beyond the crossover frequency thus it is neglected.

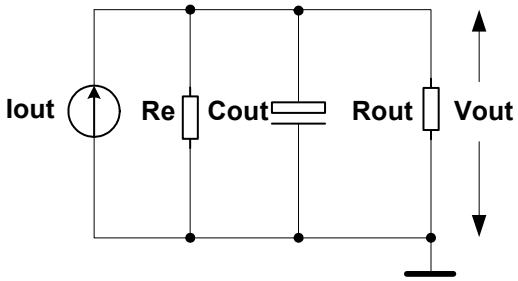


Figure 20 Power stage modeling

A few algebraic manipulations would show that the shunt resistor Re always equals the DC load resistance Rout, thus it changes depending on the power delivered by the system. There are two kinds of load in the application. Two cases will give a different result in case of resistive load or constant power load. For purely resistive load, the AC load resistance equals Ro. In case of constant power load like additional isolated PWM DC/DC converter, the AC load resistance is equal to -Ro (if the DC bus decreases, the current demanded of the PFC increases. hence the negative sign is shown.). As a result, the parallel combination with Re tends to infinity and the two resistances cancel. The current source drives only the output capacitor. The result is summarized as below:

$$\frac{\Delta V_{out}}{\Delta I_{out}} = \begin{cases} \dfrac{R_{out}}{2(1+s\cdot\dfrac{R_{out}C_{out}}{2})} & \text{Resistive Load} \\ \dfrac{1}{sC_{out}} & \text{Constant Power Load} \end{cases} \quad (45)$$

In this application note, the calculation is only carried out for constant power load situation

3.3.1.2 ΔI_{out} / ΔI_{L_rms}

The current source Iout can be characterized with the following considerations as shown in Figure 21. The low frequency component of the boost diode current is found by averaging the discharge portion of the inductor current over a given switching cycle. The low frequency current, averaged over a mains half-cycle yields the DC output current Iout:

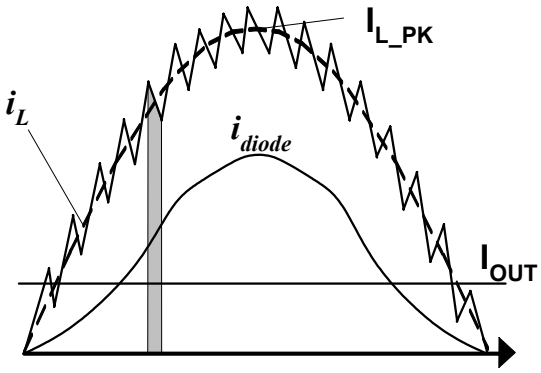


Figure 21 The simplification and characterization for I_{out} / I_{L_rms}

$$I_{out} = \frac{1}{\pi}\int_0^{\pi}(1-D_{on})I_{L\_PK}Sin\alpha d\alpha = \frac{2V_{inrms}I_{L\_rms}}{\pi V_{out\_AVE}}\int_0^{\pi}(Sin\alpha)^2 d\alpha = \frac{V_{inrms}I_{L\_rms}}{V_{out\_AVE}} \quad (46)$$

So,

$$\frac{\Delta I_{out}}{\Delta I_{L\_rms}} = \frac{V_{inrms}}{V_{out\_AVE}} \quad (47)$$

where, Don is the switch duty cycle; α is the instantaneous phase angle of the mains voltage, Vinrms is the input RMS voltage value, I_{L_PK} is choke current sinewave peak value and V_{out_AVE} is the averaging bulk DC output voltage.

In case of constant power load, the transfer function of $G_3(s)$ is:

$$G_3(s) = \frac{\Delta V_{out}}{\Delta I_{L\_rms}} = \frac{\Delta V_{out}}{\Delta I_{out}}\cdot\frac{\Delta I_{out}}{\Delta I_{L\_rms}} = \frac{V_{inrms}}{V_{out\_AVE}}\cdot\frac{1}{sC_{out}} \quad (48)$$

3.3.2 Small signal transfer function of $\Delta V_{out}/\Delta(M_1M_2)$ for voltage loop analysis

There is a internal feedback from Vout to $G_2(s)$. this inner loop has to be solved to obtain the transfer function of $\Delta V_{out}/\Delta$(M1M2). Rewrite the equation (43) at input voltage RMS point:

$$I_{L\_rms} = \frac{K_{FQ}M_1M_2V_{inrms}}{K_1R_{sense}V_{out}} \quad (49)$$

making a perturbation on I_{L_rms}, (M_1M_2), V_{out}, then

$$\Delta I_{L\_rms} = \frac{I_{L\_rms}}{M_1 M_2}\Delta(M_1 M_2) - \frac{I_{L\_rms}}{V_{out\_AVE}}\Delta V_{out} \tag{50}$$

replacing ΔI_{L_rms} by $\Delta V_{out}/G_3(s)$ according to voltage loop block diagram,

$$\frac{\Delta V_{out}}{G_3(s)} = \frac{I_{L\_rms}}{M_1 M_2}\Delta(M_1 M_2) - \frac{I_{L\_rms}}{V_{out\_AVE}}\Delta V_{out} \tag{51}$$

then the transfer function of dV_{out}/dV_{comp} is

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{\frac{V_{out\_AVE}^{\ 2} C_{out}}{I_{L\_rms} V_{inrms}}s + 1} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{\frac{K_1 R_{sense} V_{out\_AVE}^{\ 3} C_{out}}{K_{FQ} M_1 M_2 V_{inrms}^{\ 2}}s + 1} \tag{52}$$

With $f_{23} = \dfrac{1}{2\pi \dfrac{K_1 R_{sense} V_{out\_AVE}^{\ 3} C_{out}}{K_{FQ} M_1 M_2 V_{inrms}^{\ 2}}}$,

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{1 + \frac{s}{2\pi f_{23}}} \tag{53}$$

3.3.3 Nonlinear block $G_{NON}(s)$

The Vcomp voltage is sent to nonlinear gain block. The output of nonlinear is two internal variables, M1 and M2. The two variables are used to define boost choke current amplitude I_L as in equation (43). The characteristic of nonlinear gain block is shown in Table 2 and Figure 22. The small signal gain between Δ(M1*M2) and ΔVcomp can be derived as well at different operating point.

Vcomp	M1	M2	M1*M2
0.00	4.686E-02	4.964E-04	2.326E-05
0.25	4.685E-02	7.072E-04	3.313E-05
0.50	4.665E-02	1.199E-03	5.595E-05
0.75	4.685E-02	3.292E-03	1.542E-04
1.00	4.823E-02	3.224E-02	1.555E-03
1.25	8.153E-02	1.075E-01	8.766E-03
1.50	1.261E-01	1.921E-01	2.423E-02
1.75	1.901E-01	2.796E-01	5.316E-02
2.00	2.747E-01	3.686E-01	1.013E-01
2.25	3.768E-01	4.590E-01	1.729E-01
2.50	4.884E-01	5.523E-01	2.697E-01
2.75	5.992E-01	6.539E-01	3.918E-01
3.00	6.992E-01	7.794E-01	5.449E-01
3.25	7.816E-01	9.669E-01	7.557E-01
3.50	8.443E-01	1.287E+00	1.087E+00
3.75	8.888E-01	1.802E+00	1.601E+00
4.00	9.184E-01	2.442E+00	2.243E+00
4.25	9.339E-01	2.911E+00	2.719E+00

4.50	9.350E-01	2.911E+00	2.722E+00
4.75	9.351E-01	2.911E+00	2.722E+00
5.00	9.351E-01	2.911E+00	2.722E+00

Table 2 nonlinear block characteristic data

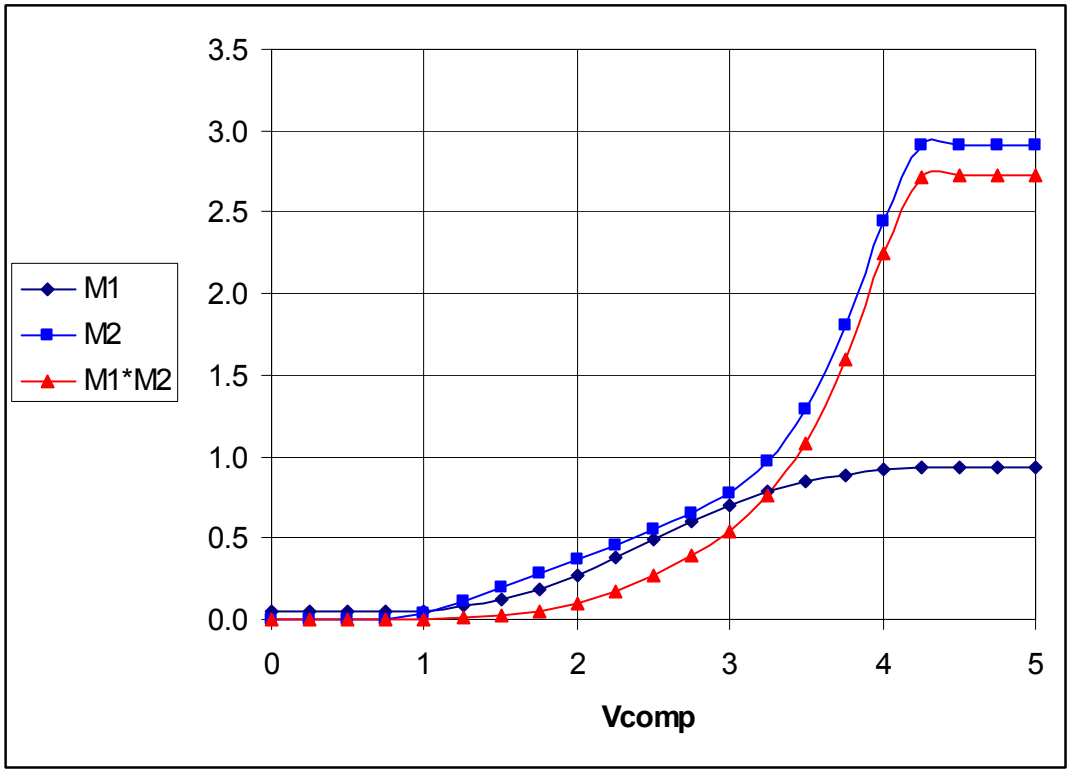


Figure 22 The characteristics of nonlinear block

3.3.4 Error Amplifier compensation $G_1(s)$

The circuit of error amplifier compensation circuit is shown in Figure 23. The sensing voltage Vsense is compared to internal reference voltage 3V typical. The difference between Vsense and internal reference is sent to transconductance error amplifier and converted to a current source to charge or discharge the RC components in Vcomp Pin.

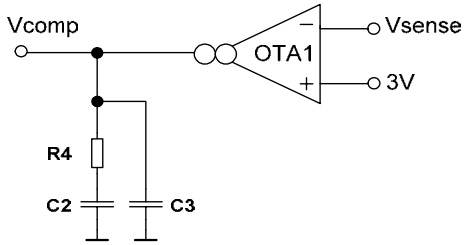


Figure 23 Error Amplifier compensation $G_1(s)$

The transfer function is:

$$G_1(s) = \frac{\Delta V_{comp}}{\Delta V_{sense}} = \frac{\Delta V_{comp}}{\Delta I_{OTA1}} \cdot \frac{\Delta I_{OTA1}}{\Delta V_{sense}} = \frac{1 + sR_4C_2}{(C_2 + C_3)s(1 + s\frac{R_4C_2C_3}{C_2 + C_3})} \cdot g_{OTA1} \quad (54)$$

where, g_{OTA1} is the trans-conductance of OTA1, 42uS typically for ICE2PCS02.

With $f_{CZ} = \frac{1}{2\pi R_4 C_2}$ and $f_{CP} = \frac{1}{2\pi \frac{R_4 C_2 C_3}{C_2 + C_3}}$,

$$G_1(s) = \frac{g_{OTA1}(1 + s/2\pi f_{CZ})}{(C_2 + C_3)s(1 + s/2\pi f_{CP})} \quad (55)$$

The pole and zero are to regulate the overall voltage loop with the cross-over frequency below 100Hz and create the phase margin for the loop stability.

3.3.5 Feedback $G_4(s)$

The Feedback block is a simple voltage divider to monitor the bulk capacitor output voltage. The circuit is shown in Figure 24.

$$G_4(s) = \frac{\Delta V_{sense}}{\Delta V_{out}} = \frac{R_2}{R_1 + R_2} \quad (56)$$

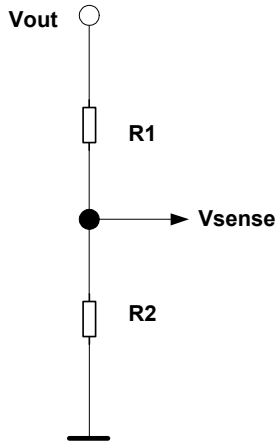


Figure 24 bulk voltage sensing divider

3.3.6 Overall Open Loop Transfer Function $G_V(s)$

With combining all of the blocks above, the overall open loop gain for voltage loop is equal to:

$$G_V(s) = G_1(s)G_{NON}(s)G_{23}(s)G_4(s) \quad (57)$$

Due to PF requirement, inherent PFC dynamic voltage loop compensation is always implemented with low bandwidth in order not to make the response for $2*f_L$ ripple. For example, for 50Hz AC line input, PFC voltage loop bandwidth is normally set below 20Hz. The compensation circuit R4, C2 and C3 are used to optimize the loop gain and phase margin.

3.3.7 Enhance dynamic response

As mentioned in Section 4.6, the inherent low bandwidth of voltage loop in PFC application will lead to slow response in case of sudden load step and result in large output overshoot or drop. Enhance dynamic response feature is integrated in ICE2PCS02 to have a fast response in the case of load step. The voltage loop with including enhance dynamic response block is shown in Figure 25.

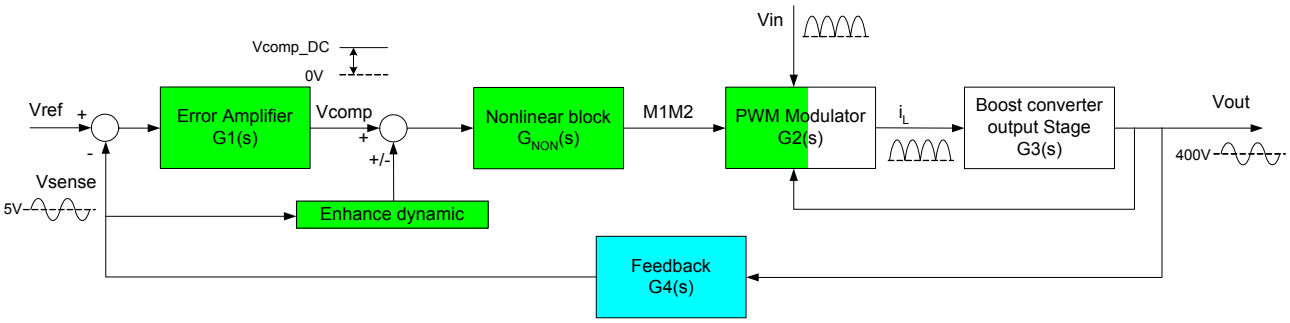


Figure 25 voltage loop block diagram including enhance dynamic response

When Vsense voltage variation is within -5% to +5% of nominal value, there is no function of enhance dynamic response block. However, when Vsense variation is out of such +/-5% range, enhance block will add offset voltage on top of Vcomp voltage to influence the current amplitude.

The timing diagram of enhance dynamic response operation is shown in Figure 26 with sudden load jump situation. It can be seen that during enhance dynamic operation, the high current of boost choke is delivered for fast response. Within half sinusoidal period, when Vsense operating around the boundary of -5% threshold, the first part of boost choke current follows high amplitude profile due to enhance mode offset and the rest of boost choke current come back to low amplitude profile without enhance mode offset. When Vsense voltage is pulled back within +/-5% range, enhance dynamic offset disappear and boost choke current waveform will stay as perfect sinusoidal shape.

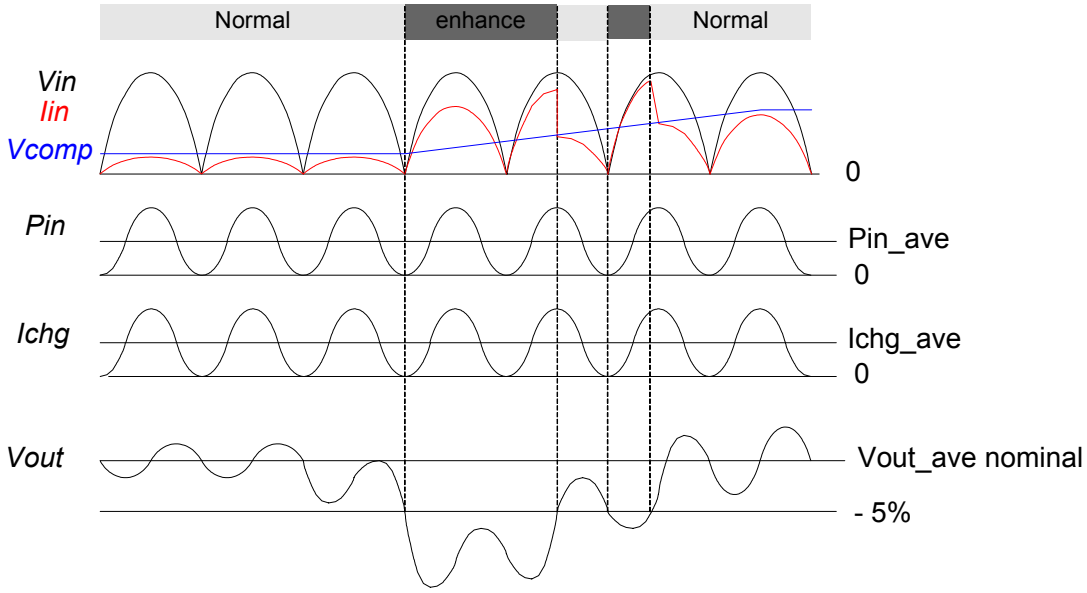


Figure 26 timing diagram for enhance dynamic operation

3.4 Design Example

Assuming a 300W application with universal input AC voltage 85~265VAC,

constant power load
efficiency=90%

Vout=400VDC
Cout=220uF/450V
f_{SW}=125kHz
Rsense=0.1ohm
Boost choke inductance L=1.2mH (please note that the inductance may change at different choke current)
Vsense divider: R1=390kohm*2=780kohm, R2=6kohm

3.5 Vcomp and M1, M2 value at full load condition

(1) 85VAC:

RMS AC input current under full load:

$$I_{L\_rms\_85} = \frac{P_{out}}{\eta \cdot V_{inrms\_85}} = \frac{300}{0.9 \cdot 85} = 3.92A \tag{58}$$

From equation (43), With $K_{FQ} = 4.34$ and $K_1 = 4$ from the ICE2PCS02 Datasheet,

$$M_1 M_2\big|_{85VAC} = \frac{I_{L\_rms\_85} K_1 R_{sense} V_{out}}{K_{FQ} V_{inrms\_85}} = \frac{3.92 \cdot 4 \cdot 0.1 \cdot 400}{4.34 \cdot 85} = 1.70 \tag{59}$$

From table 2 and Figure 22, it can be obtained

Vcomp	M1	M2	M1*M2
3.75	8.888E-01	1.802E+00	1.601E+00
4.00	9.184E-01	2.442E+00	2.243E+00

With Linear approximation:

$$V_{comp\_85} = V_{comp\_1} + \frac{M_1 M_2\big|_{85VAC} - M_1 M_2\big|_{Vcomp\_1}}{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}} \cdot (V_{comp\_2} - V_{comp\_1}) \tag{60}$$

$$V_{comp\_85} = 3.75 + \frac{1.70 - 1.601}{2.243 - 1.601} \cdot (4 - 3.75) = 3.79V$$

$$M_1\big|_{85VAC} = M_{1\_1} + \frac{M_{1\_2} - M_{1\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_85} - V_{comp\_1}) \tag{61}$$

$$M_1\big|_{85VAC} = 0.889 + \frac{0.918 - 0.889}{4 - 3.75} \cdot (3.79 - 3.75) = 0.894$$

$$M_2\big|_{85VAC} = M_{2\_1} + \frac{M_{2\_2} - M_{2\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_85} - V_{comp\_1}) \tag{62}$$

$$M_2\big|_{85VAC} = 1.802 + \frac{2.442 - 1.802}{4 - 3.75} \cdot (3.79 - 3.75) = 1.91$$

The small signal gain of nonlinear block is

$$G_{NON}(s)\big|_{85VAC} = \frac{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}}{V_{comp\_2} - V_{comp\_1}} = \frac{2.243 - 1.601}{4 - 3.75} = 2.568 \tag{63}$$

The inherent pole of f_{23} is

$$f_{23}\big|_{85VAC} = \frac{1}{2\pi \frac{K_1 R_{sense} V_{out\_AVE}{}^3 C_{out}}{K_{FQ} \cdot (M_1 M_2)\big|_{85VAC} \cdot V_{inrms\_85}{}^2}} = 1.54Hz \tag{64}$$

(2) 265VAC

RMS AC input current under full load:

$$I_{L\_rms\_265} = \frac{P_{out}}{\eta \cdot V_{inrms\_265}} = \frac{300}{0.9 \cdot 265} = 1.257A \tag{65}$$

From equation (43),

$$M_1 M_2\big|_{265VAC} = \frac{I_{L\_rms\_265} K_1 R_{sense} V_{out}}{K_{FQ} V_{inrms\_265}} = \frac{1.257 \cdot 4 \cdot 0.1 \cdot 400}{4.34 \cdot 265} = 0.175 \tag{66}$$

From table 2 and Figure 22, it can be obtained

Vcomp	M1	M2	M1*M2
2.25	3.768E-01	4.590E-01	1.729E-01
2.50	4.884E-01	5.523E-01	2.697E-01

With Linear approximation:

$$V_{comp\_265} = V_{comp\_1} + \frac{M_1 M_2\big|_{265VAC} - M_1 M_2\big|_{Vcomp\_1}}{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}} \cdot (V_{comp\_2} - V_{comp\_1})$$

$$V_{comp\_265} = 2.25 + \frac{0.175 - 0.1729}{0.2697 - 0.1729} \cdot (2.5 - 2.25) = 2.255V \tag{67}$$

$$M_1\big|_{265VAC} = M_{1\_1} + \frac{M_{1\_2} - M_{1\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_265} - V_{comp\_1})$$

$$M_1\big|_{265VAC} = 0.3768 + \frac{0.4884 - 0.3768}{2.5 - 2.25} \cdot (2.266 - 2.25) = 0.386 \tag{68}$$

$$M_2\big|_{265VAC} = M_{2\_1} + \frac{M_{2\_2} - M_{2\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_265} - V_{comp\_1})$$

$$M_2\big|_{265VAC} = 0.459 + \frac{0.5523 - 0.459}{2.5 - 2.25} \cdot (2.255 - 2.25) = 0.461 \tag{69}$$

The small signal gain of nonlinear block is

$$G_{NON}(s)\big|_{265VAC} = \frac{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}}{V_{comp\_2} - V_{comp\_1}} = \frac{0.2697 - 0.1729}{2.5 - 2.25} = 0.3872 \tag{70}$$

The inherent pole of f_{23} is

$$f_{23}\big|_{265VAC} = \frac{1}{2\pi \frac{K_1 R_{sense} V_{out\_AVE}{}^3 C_{out}}{K_{FQ} \cdot (M_1 M_2)\big|_{265VAC} \cdot V_{inrms\_265}{}^2}} = 1.54Hz \tag{71}$$

3.5.1 Current Averaging Circuit

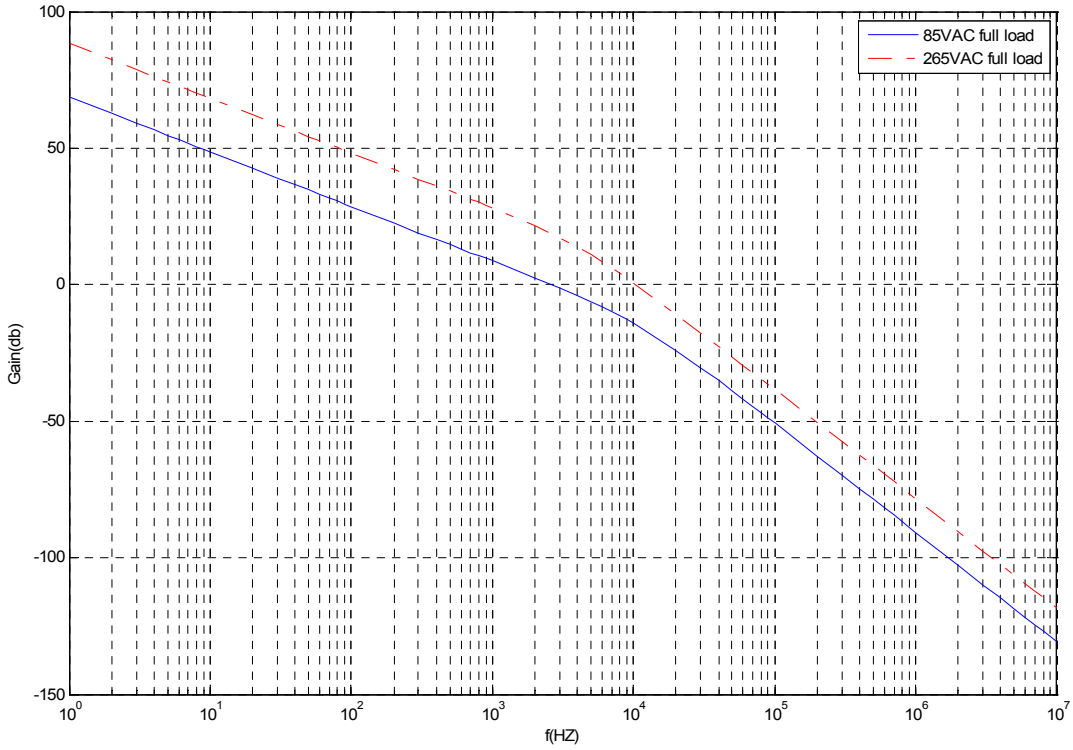
With g_{OTA2}=1.0mS from Datasheet, M1@85VAC, and assuming f_{AVE}=13kHz which is 10 times less than switching frequency 125kHz, then

$$C_{icomp} \geq \frac{g_{OTA2} M_1\big|_{85VAC}}{K_1 \cdot 2\pi f_{AVE}} = \frac{1.0E-3 \cdot 0.895}{4 \cdot 2\pi \cdot 24E3} = 3nF \tag{72}$$

Select C_{icomp}=3.3nF

3.5.2 Current Loop Regulation

Insert M1 and M2 value in equation (40). The amplitude and phase angle of $G_C(s)$ is shown in Figure 27 to verify the stability of current loop and the requirement of f_C less than switching frequency.



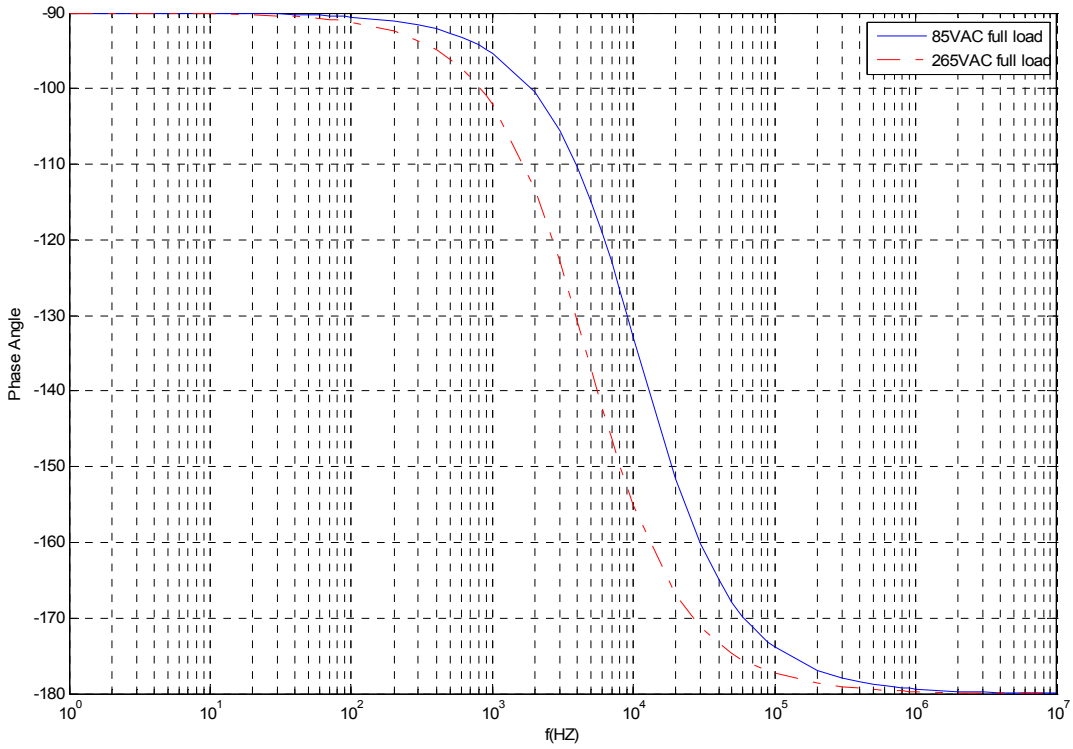


Figure 27 The bode plot and phase angle for current loop

The cross over frequency and phase margin are 3kHz and 75º for 85VAC, and 10kHz and 25º for 265VAC.

3.5.3 Voltage Loop Regulation

From the above sections, it can be obtained:

$$G_1(s) = \frac{\Delta V_{comp}}{\Delta V_{sense}} = \frac{g_{OTA1}(1 + s/2\pi f_{CZ})}{(C_2 + C_3)s(1 + s/2\pi f_{CP})} \tag{73}$$

$$G_{NON}(s) = \frac{\Delta(M_1 M_2)}{\Delta V_{comp}} \tag{74}$$

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{1 + \frac{s}{2\pi f_{23}}} \tag{75}$$

$$G_4(s) = \frac{\Delta V_{sense}}{\Delta V_{out}} = \frac{R_2}{R_1 + R_2} = \frac{6.2}{806.2}. = 0.0077 \tag{76}$$

The open loop gain for voltage loop is to times all above factors together as:

$$G_V(s) = G_1(s) G_{NON}(s) G_{23}(s) G_4(s)$$

$G_1(s)$ is used to provide enough phase margin and also limit the bandwidth below 20HZ. R4, C2 and C3 can be chosen as required. f_{CZ} normally select to be compensate the pole in $G_{23}(s)$. f_{CP} normally select to be 40~70Hz in order to fast put down the gain amplitude and reject the high frequency interference. In this example f_{23} is around 1.54Hz at 85VAC/ 265VAC and full load. So the initial target is: f_{CZ} is chosen to be close to 1.5Hz, and f_{CP} is chosen to be 50Hz.

C2 and C3 is calculated to obtain Gv(s) cross over frequency around 10Hz. The gain amplitude of G_{NON}*G_{23}*G_4 in 85VAC and full load is shown in Figure 28. It can be seen that at f=10Hz, the gain is about -4.52dB. So G1 should provide the gain +4.52dB at f=10Hz. Considering that C2>>C3 due to fcz<fcp and 10Hz>>1Hz=f_{CZ}, then

$$G_1(10Hz) = \frac{g_{OTA1} \, 10Hz/1Hz}{C_2 \cdot 2\pi \cdot 10Hz} = +4.52dB$$
$$C_2 = \frac{39 \cdot 10^{-6} \cdot \frac{10Hz}{1Hz}}{10^{4.52/20} \cdot 2\pi \cdot 10Hz} = 3.69\mu F \tag{77}$$

3.97uF is not common for ceramic type capacitor. So select C_2=1uF, then f_{CZ} is recalculated as:

$$G_1(10Hz) = \frac{g_{OTA1}\sqrt{1+(10Hz/f_{CZ})^2}}{C_2 \cdot 2\pi \cdot 10Hz} = +4.52dB$$

$$f_{CZ} = \frac{10Hz}{\sqrt{\left(\frac{1\mu F \cdot 10^{4.52/20} \cdot 2\pi \cdot 10Hz}{39 \cdot 10^{-6}}\right)^2 - 1}} = 4.30Hz \quad (78)$$

according to $f_{CZ} = \frac{1}{2\pi R_4 C_2} = 4.30Hz$ then

$$R_4 = \frac{1}{2\pi \cdot 4.30Hz \cdot C_2} = 37k\Omega \quad (79)$$

select R4=33kΩ, and $f_{CP} = \frac{1}{2\pi \frac{R_4 C_2 C_3}{C_2 + C_3}} \approx \frac{1}{2\pi R_4 C_3} = 50Hz$

$$C_3 = \frac{1}{2\pi \cdot 50Hz \cdot R_4} = 96.5nF \quad (80)$$

select C3=100nF

The gain amplitude and phase angle of overall voltage loop $G_V(s)$ at 85VAC and 265VAC in full load condition is shown in Figure 28 and Figure 29. At 85VAC, the cross over frequency f_V is around 9.5Hz and the phase margin is about 63º. At 265VAC, the cross over frequency f_V is around 14Hz and the phase margin is about 62º.

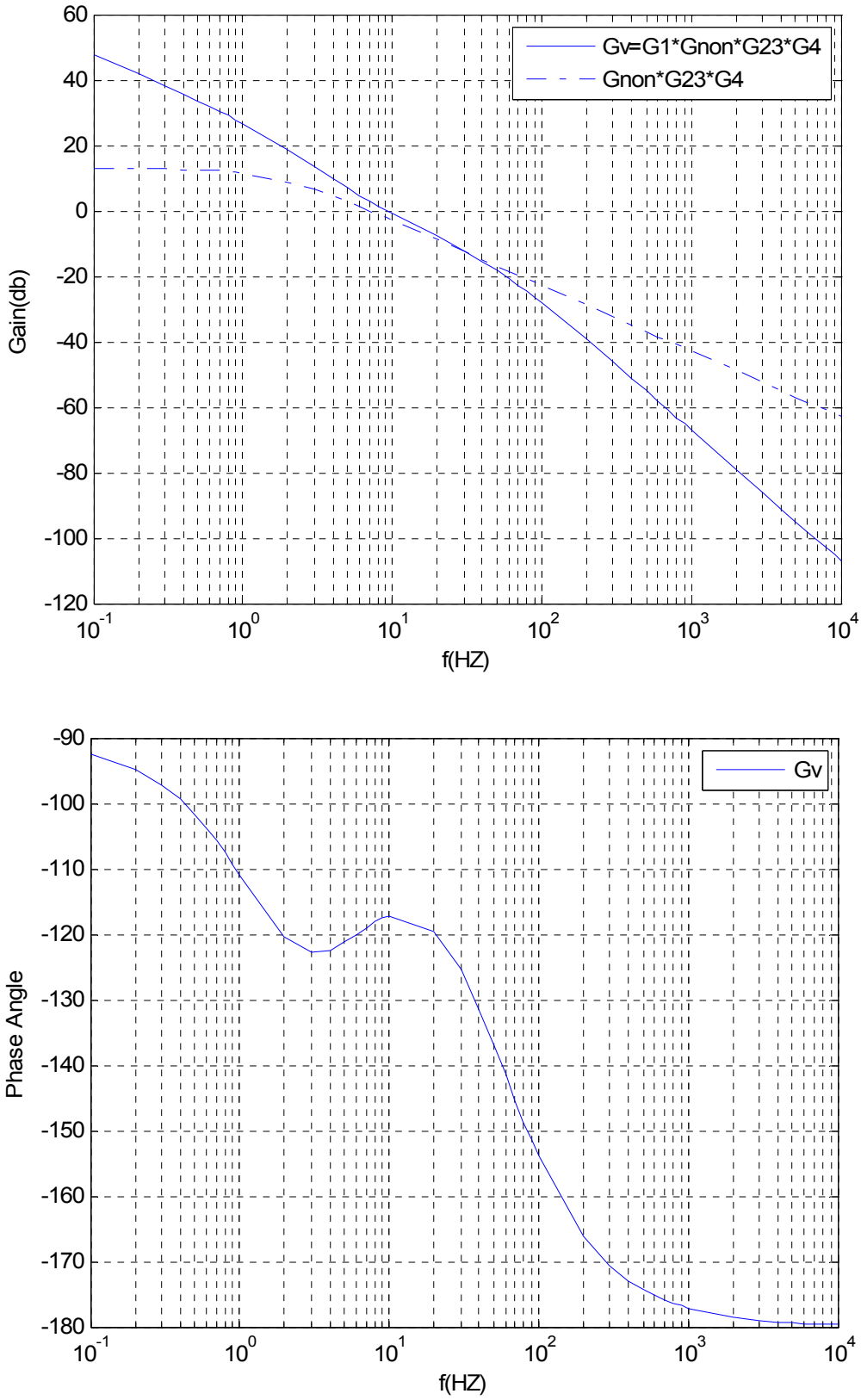


Figure 28 the bode plot and phase angle for voltage loop at 85VAC and full load

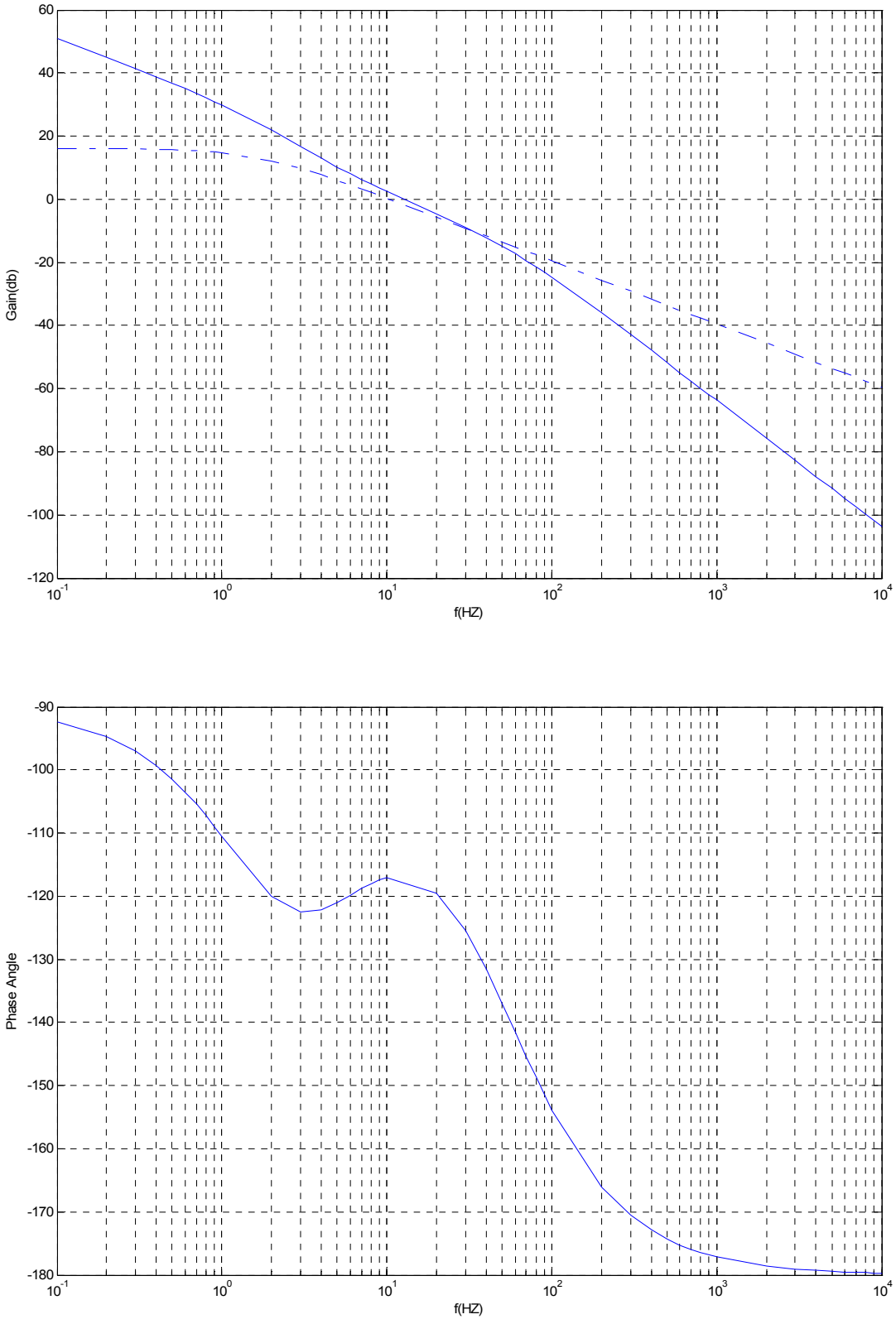


Figure 29 The bode plot and phase angle for voltage loop at 265VAC and full load

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