1. Description

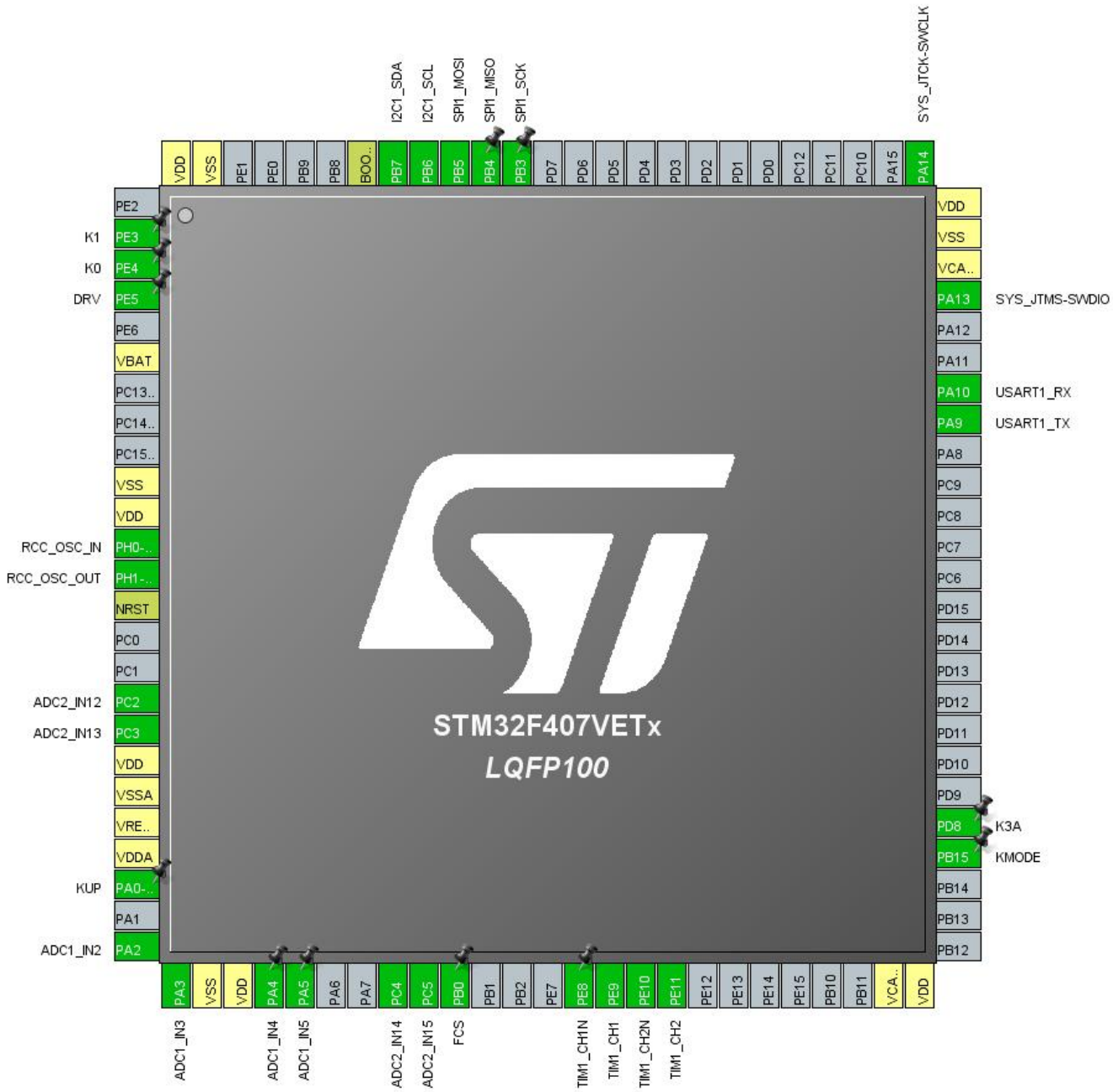
1.1. Project

Project Name	IICOLED
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	05/31/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



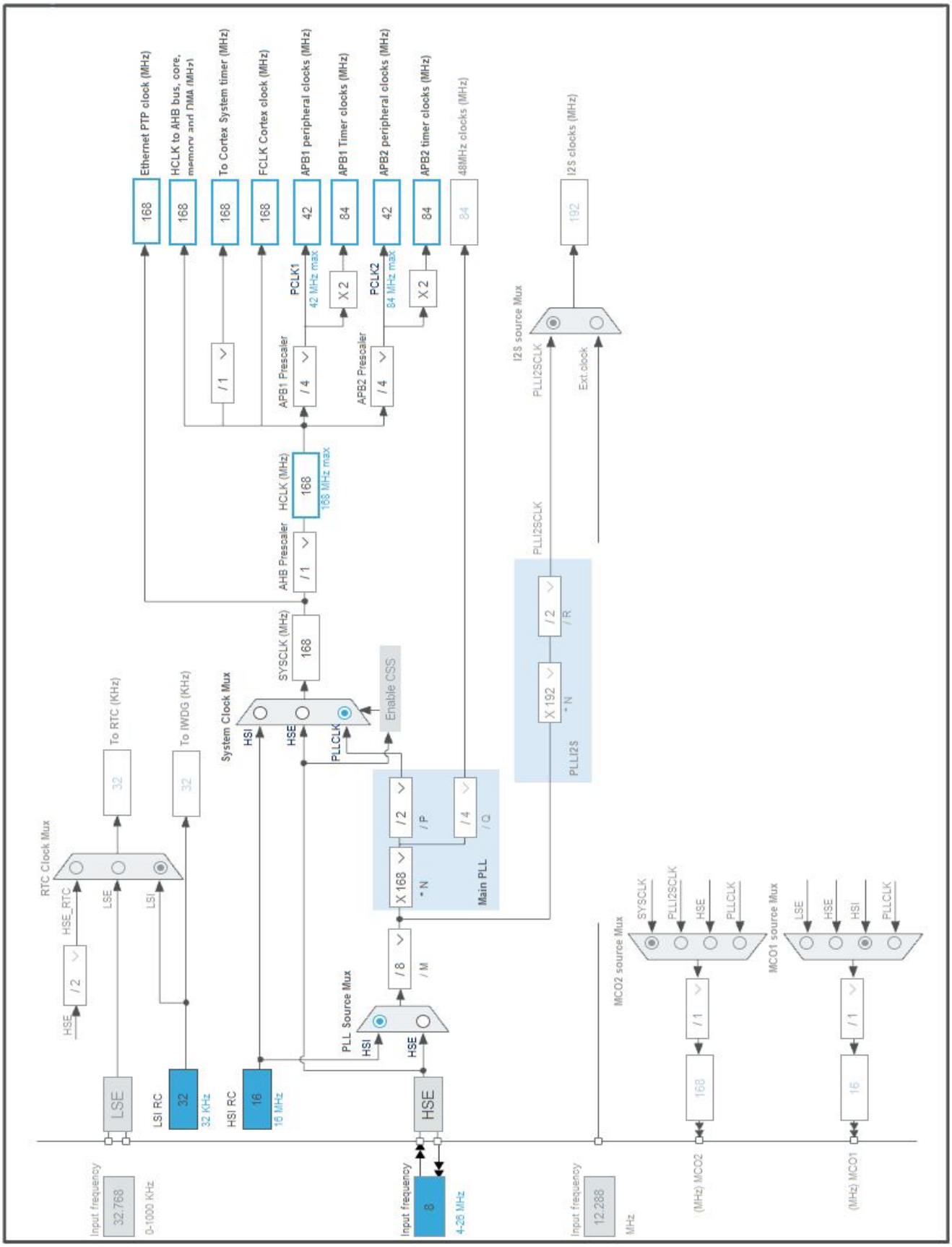
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3	I/O	GPIO_EXTI3	K1
3	PE4	I/O	GPIO_EXTI4	K0
4	PE5 *	I/O	GPIO_Output	DRV
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
17	PC2	I/O	ADC2_IN12	
18	PC3	I/O	ADC2_IN13	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	GPIO_EXTI0	KUP
25	PA2	I/O	ADC1_IN2	
26	PA3	I/O	ADC1_IN3	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	
30	PA5	I/O	ADC1_IN5	
33	PC4	I/O	ADC2_IN14	
34	PC5	I/O	ADC2_IN15	
35	PB0 *	I/O	GPIO_Output	FCS
39	PE8	I/O	TIM1_CH1N	
40	PE9	I/O	TIM1_CH1	
41	PE10	I/O	TIM1_CH2N	
42	PE11	I/O	TIM1_CH2	
49	VCAP_1	Power		
50	VDD	Power		
54	PB15 *	I/O	GPIO_Input	KMODE
55	PD8 *	I/O	GPIO_Input	K3A
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
89	PB3	I/O	SPI1_SCK	
90	PB4	I/O	SPI1_MISO	
91	PB5	I/O	SPI1_MOSI	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	IICOLED
Project Folder	E:\Users\Nonoki\Desktop\\05.12VDC Power
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN2

mode: IN3

mode: IN4

mode: IN5

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	**15 Cycles ***
Rank	**2 ***
Channel	**Channel 3 ***
Sampling Time	**15 Cycles ***
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**15 Cycles ***
Rank	**4 ***
Channel	**Channel 5 ***
Sampling Time	**15 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN12

mode: IN13

mode: IN14

mode: IN15

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 12
Sampling Time	3 Cycles
Rank	**2 ***
Channel	**Channel 13 ***
Sampling Time	3 Cycles
Rank	**3 ***
Channel	**Channel 14 ***
Sampling Time	3 Cycles
Rank	**4 ***
Channel	**Channel 15 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.5. SPI1

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**21.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.7. TIM1

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1680-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	**2 ***

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.8. TIM5

mode: Clock Source

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. TIM9

mode: Clock Source

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

7.10. TIM12

mode: Clock Source

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1200-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC2	ADC2_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC2_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC2_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	K1
	PE4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	K0
	PE5	GPIO_Output	Output Push Pull	**Pull-down ***	**Very High ***	DRV
	PA0-WKUP	GPIO_EXTI0	**External Interrupt Mode with Falling edge trigger detection**	**Pull-down ***	**n/a**	KUP
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	FCS
	PB15	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KMODE
	PD8	GPIO_Input	Input mode	**Pull-up ***	**n/a**	K3A

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***
ADC2	DMA2_Stream2	Peripheral To Memory	**Very High ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

ADC2: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	6	0
EXTI line3 interrupt	true	7	0
EXTI line4 interrupt	true	7	0
TIM1 break interrupt and TIM9 global interrupt	true	3	0
TIM1 capture compare interrupt	true	2	0
TIM8 break interrupt and TIM12 global interrupt	true	4	0
TIM5 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report