MS6908

Synchronous Rectifier Controller

DESCRIPTION

MS6908 is a synchronous rectifier controller, used for the secondary side rectification of isolation topologies, such as Flyback, Forward, Half Bridge, Full Bridge and LLC converter. By driving an external MOSFET, MS6908 is able to significantly improve the efficiency comparing with the conventional Diode rectifier.

When MS6908 senses V_{DS} of MOSFET less than -300mV, it turns on the MOSFET. Once the V_{DS} is greater than -10mV, MS6908 turns off the MOSFET.

MS6908 supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant.

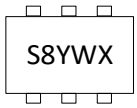
FEATURES

- Supports DCM, Quasi-Resonant, CrCM and CCM operation
- Support the isolation topologies, such as Flyback, Forward, Half Bridge and Full Bridge converter
- Output voltage directly supply VCC
- Low quiescent current
- Under-voltage protection
- Fast driver capability for CCM operation

APPLICATIONS

- Flyback and LLC converters
- Adaptor
- LCD and PDP TV

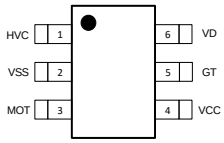
PACKAGE INFORMATION



SOT23-6

Y: Year code
W: Week code
X: Lot No.

PIN INFORMATION

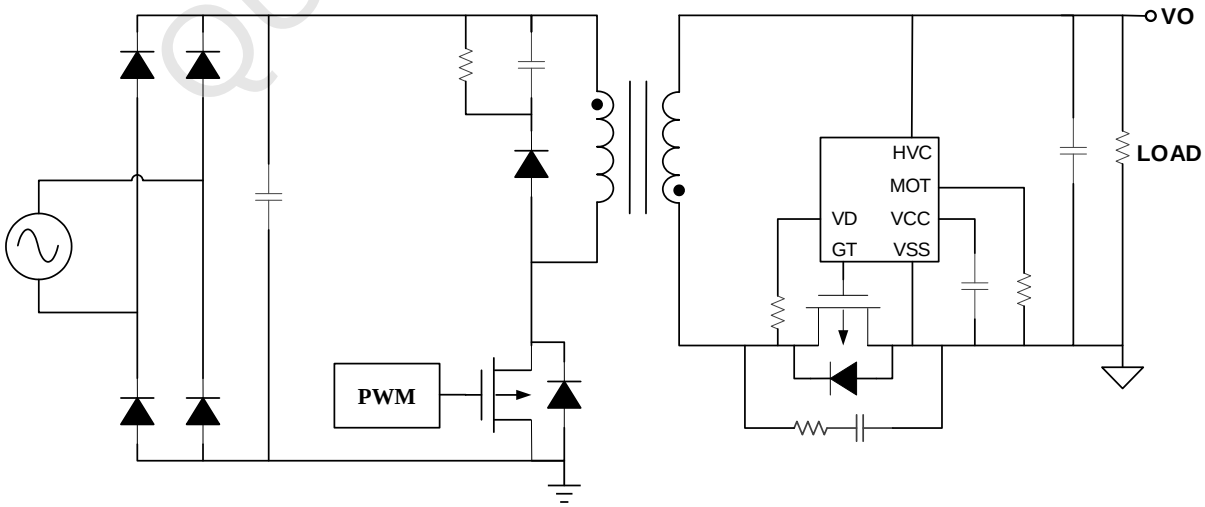


ORDER INFORMATION

MS6908□□□
- Packing Code
- Temperature Code
- Package Code

P/N	Package	Packing
MS6908TDT	SOT23-6	Tape Reel, 3000

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

VD Pin……-0.7 ~ 150.0V
HVC Pin……-0.3 ~ 30.0V
Other Pins……-0.3 ~ 6.5V
ESD Susceptibility
HBM (Human Body Model) ……2000V
MM (Machine Model) ……400V
CDM (Charge Device Model) ……500V

Operating Temperature Range……-40 ~ +125°C
Storage Temperature Range……-65 ~ +150°C
Junction Temperature……145°C
Lead Temperature (Soldering, 10sec) ……260°C
SOT23-6 Thermal Resistance θ_{JA} / θ_{JC}…220 / 130°C/W

RESOMMENDED OPERATING CONDITIONS

VD……4.5 ~ 140V
HVC……4.5 ~ 20V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Clamp Voltage	V_{CC_CLP}	V_D = 40V, V_{CC}=2.2uF		6		V
VCC Startup voltage	V_{CC_ON}			4.2		V
VCC UVLO Threshold	V_{UV}			4.0		V
Operation Current (Switching)	I_D	GT = 5nF, F = 100KHz		3.2		mA
Operation Current (GT On)	I_{CC}	GT = 5nF, V_{CC} = 2.2uF		1.1		mA
Quiescent Current	I_Q	V_{CC} = 4.5V, V_{CC} = 2.2uF		32		μA
Gate Turn on Threshold	V_{D_ON}			-300		mV
Gate Turn off Threshold	V_{D_OFF}			-10		mV
Gate Turn off Threshold in MOT	V_{D_MOT}			70		mV
Gate Turn on Voltage	V_{GT}	V_D = 32V, V_{CC} = 2.2uF	V_{CC}-1	V_{CC}		V
Gate Pull up current	I_{GU}			0.65		A
Gate Pull down current	I_{GD}			4.7		A
Gate Minimum on Time	T_{ON_MIN}	R_{MOT} = 100KΩ		1.3		μA
Gate Minimum off Time	T_{OFF_MIN}			630		nS
MOSFET Turn-on total delay	T_{DON}	R_{GATE} = 0Ω, C_{LOAD} = 5nF		110		nS
		R_{GATE} = 0Ω, C_{LOAD} = 10nF		130		
MOSFET Turn-off total delay	T_{DOFF}	R_{GATE} = 0Ω, C_{LOAD} = 5nF		22.4		nS
		R_{GATE} = 0Ω, C_{LOAD} = 10nF		32.4		
VCC Charge Current	I_{CC_CHG}	V_D = 32V, V_{CC} = 3.5V		20		mA
VD Control Voltage	V_{D_REG}			-40		mV
VD Control Voltage MAX	$V_{D\_REG\_MAX}$			-170		mV
HVC Enable Charge Voltage	V_{HVC_EN}	V_{CC} = 3V, V_D = 0V		4.3		V
HVC Charge Current	I_{HVC_CHG}	V_D = 0V, V_{CC} = 3.5V, V_{HVC} = 5V		28		mA
HVC Short-circuit Detection Voltage	V_{HVC_UV}			2.1		V

Notes:

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device these are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for textured periods my affect device reliability.

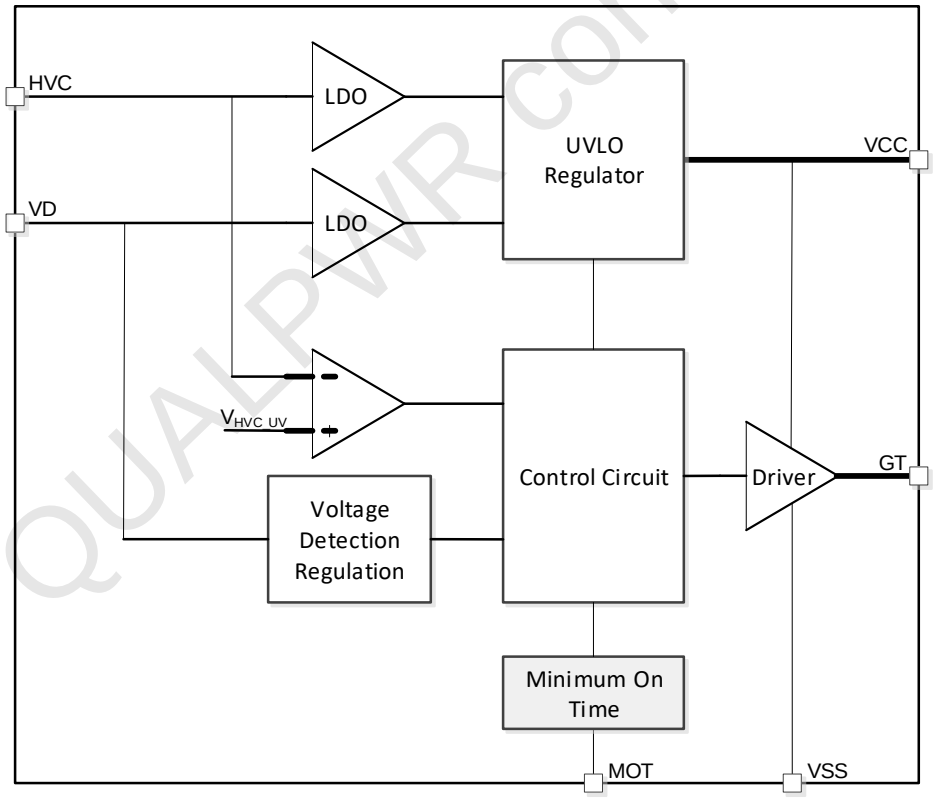
2) The parameters depend on the design and pass the functional test in mass production.

3) Measured on JESD51-7, 4-layer PCB.

PIN DESICRIPTION

PIN	NAME	DESCRIPTION
1	HVC	Output Voltage Sensing and Charging to VCC
2	VSS	Ground. VSS is used as a MOSFET source sense reference for VD
3	MOT	Set the minimum on-time, floating the pin means 1.3uS
4	VCC	Power supply. Bypass a Capacitor Between VCC and VSS
5	GT	Drive the External NMOSFET
6	VD	External Power MOSFET Drain Voltage Sensing. Charging to VCC

BLOCK DIAGRAM



OPERATION

MS6908 is a synchronous rectifier controller which combined with external MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in flyback converter.

Startup

During the startup period, when the VCC is lower than startup voltage, the external MOSFET is turned off. The current flows though body diode before the VCC

reaches to the startup voltage V_{CC_ON}.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage V_{CC_ON}, the parts is activated again.

LDO Charging Logic

MS6908 have two internal LDO to charge the VCC pin. When HVC is lower than 4.3V, MS6908 can power itself through the internal LDO connected to VD pin during the SR turn-off period, which means primary the primary side MOSFET is turned on and SW presents a positive voltage. A capacitor between VCC and VSS is required to store the energy and supply to IC during the SR turn-on period.

The other internal LDO is connected from HVC to VCC, it charges VCC pin when HVC is higher than 4.3V.

Turn Off Phase

After synchronous MOSFET conducting, once the voltage V_D touches the MOSFET turn off threshold (-10mV), the gate is pulled to low after a turn off delay time T_{DOFF}. A 630nS blanking time is necessary to avoid error trigger.

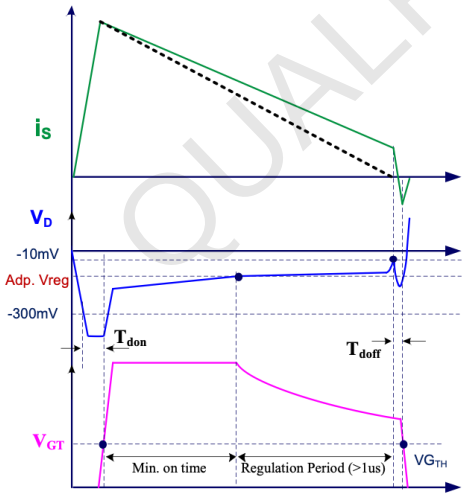


Figure 1. Turn on delay and turn off delay

Conducting Phase

When the synchronous MOSFET is turn on, the drain source voltage VD it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the VD to an internal threshold (typical -40mV) after the synchronous MOSFET turn on. When the VD is lower than -40mV, the gate keeps its maximum voltage. And the synchronous MOSFET is fully on.

The control circuit contains a minimum on time function. The VD voltage may have a parasitic ring when the synchronous MOSFET turns on. So a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered. During the minimum time, the gate can still be turned off if VD touches a positive threshold value, +70mV.

Turn Off Phase

After synchronous MOSFET conducting, once the voltage VD touches the MOSFET turn off threshold (-10mV), the gate is pulled to low after a turn off delay time T_{DOFF}. A 630nS blanking time is necessary to avoid error trigger.

Minimum on-time (MOT)

MOT stands for the minimum on time of synchronous MOSFET or the maximum duty cycle of primary MOSFET, The MOT can be adjusted by a resistor connected to MOT pin. Floating MOT will result in a maximum on time (~1.3uS), and shorting MOT to VSS turns out to a minimum on time (~700nS) for high frequency applications.

Output Voltage Detection

The MS6908 has output voltage detection function via HVC pin. To avoid the gate error turn on during starting-up period, the whole SR control logic is disabled when the HVC voltage is lower than 2.1V. VCC is charged from HVC pin when HVC is higher than 4.3V to save power loss caused by the LDO when charging from VD pin to VCC pin.

Typical System Implementations

Figure 2 shows the typical system implementation for the IC power supply derived from the output voltage (VOUT), which is available in low-side rectification.

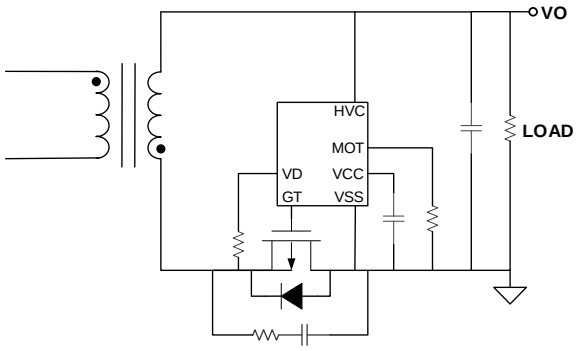


Figure 2. Low-Side Rectification

The MS6908 can support most applications, even when VO is down to 0V for low-side rectification.

If the MS6908 is used for high-side rectification, Figure 2 shows the typical system implementation. a self-supply can be achieved.

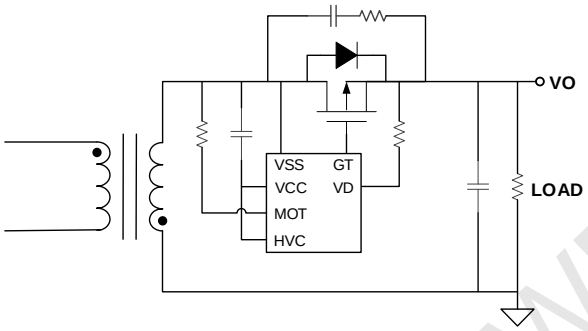


Figure 3. High-Side Rectification

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, please follow the guidelines below.

Sensing for VD/VSS

1. Make the sensing connection (VD/VSS) as close as possible to the MOSFET (drain/source).
2. Make the sensing loop as small as possible.
3. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other (see Figure 4).

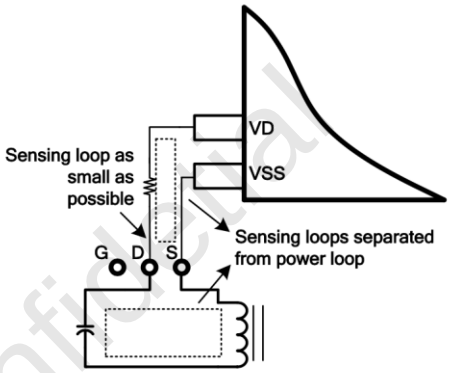


Figure 4. Voltage Sensing for VD/VSS

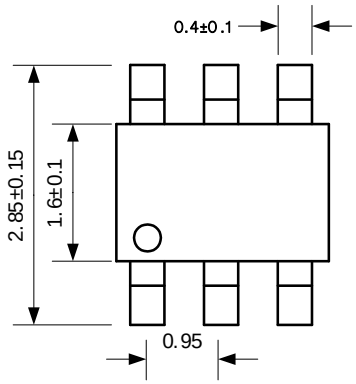
4. Place a decoupling ceramic capacitor from VCC to PGND close to the IC for adequate filtering.

Gate Driver Loop

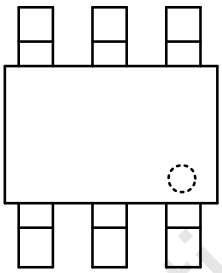
1. Make the gate driver loop as small as possible to minimize the parasitic inductance.
2. Keep the driver signal far away from the VD sensing trace on the layout.

PACKAGE DESCRIPTION

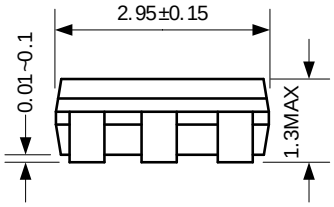
SOT23-6 Package



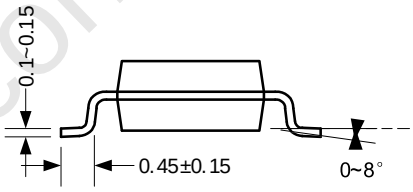
TOP VIEW



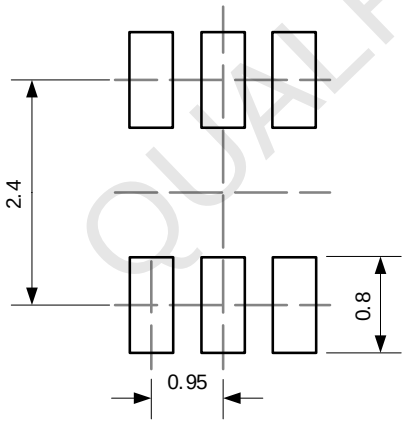
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.
6) UNFILLED TOLERANCE:±0.05.